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Low-power VLSI Design by using Dynamic-threshold Logic

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***Abstract* – Power dissipation is a serious concern for circuit designers. In the last few decades due to the ever growing demand for portable and small sized devices, integrated circuits require electronic circuit design methods to implement integrated circuits with low power consumption. The ever-growing number of transistors integrated on a chip and the increasing transistor switching speed in recent decades has enabled great performance improvement in computer systems by several orders of magnitude. Unfortunately, such phenomenal performance improvements have been accompanied by an increase in power and energy dissipation of the systems.**

A conventional CMOS logic circuit design approach depends upon charging the output capacitive nodes to the supply voltage or discharging it to the ground. This is one of the most used methods in VLSI designs. There are various techniques to design low power circuits both at system level as well as at circuit level to reduce power consumption. Partially-depleted SOI provides a Dynamic Threshold MOS transistor that may be useful in reducing static power and dynamic power. DTMOS can be used to choke off leakage current and improve performance of transistors under lower voltage conditions, but suffers from high body contact resistance, Miller capacitance, area penalties, and limited operating voltage. Driving the body with a separate conditioning signal and careful design are proposed as ways to offset the above problems and still take advantage of DTMOS. A ring oscillator has been implemented to verify the use of this technology in various configurations. This information will be helpful in the design of circuits for data path elements.

***Keywords* – DTMOS, High Body Contact Resistance, Miller Capacitance, Ring Oscillator.**

I. INTRODUCTION

The proliferation of battery-powered electronics has made low-power VLSI design an important research topic. Silicon-on-insulator technology is well suited for low-power design because of its reduced junction capacitance due to the buried oxide layer. The buried oxide also isolates the silicon under the transistor's channel. When the silicon is thick enough, as in Partially-Depleted SOI (PD-SOI), the silicon under the channel does is not depleted of charge carriers under strong inversion, leaving a fifth, body terminal that affects threshold voltage and device performance. When the body terminal is connected to the gate or driven during switching from some other signal, a Dynamic Threshold transistor (DTMOS) is created [1]. In traditional DTMOS, Figure 1(a), the gate is tied directly to the body. When the gate switches from high to low, the body also switches from high to low which sets the body-source voltage to 0V. The threshold voltage, which is dependent on the body-source voltage, is at its highest value and leakage currents are low. When the gate, and consequently the body, switches from low to high, the threshold voltage decreases with increasing source-body voltage and the drive current of the transistor increases. In summary, DTMOS provides low-leak-age and high-current transistors.

The pull-down networks of some of the inverters studied are shown in Figure 1. In inverters (a)-(e) the body switches each time the inverter switches. For inverters (f)-(i), the body switching depends on the behavior of V_{ref}, which can vary from a static reference to switching at the same frequency as the inverter. The concept of DTMOS is independent of topology since DTMOS refers to the ability to change threshold-voltage dynamically during circuit operation, regardless of how quickly that switching occurs. In this work DTMOS will refer to circuits that can dynamically change threshold voltage and "traditional DTMOS" will refer to circuits that switch the body every cycle with the gate. Floating-body gates will simply be referred to as FB-CMOS.

In order for DTMOS to be effective, the body capacitance and body resistance need to be small so that the RC time constant to charge the body is smaller than the switching period driving the body; otherwise, the body voltage will not change until after the transistor has

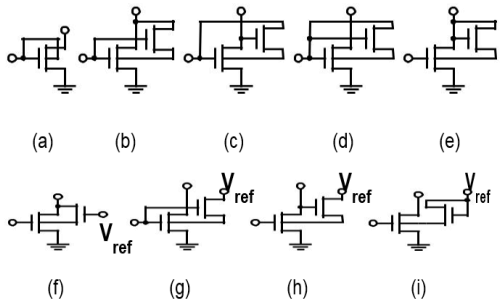

Fig. 1. DTMOS circuit configurations in the literature.

Switched which is too late to decrease the transistor's delay. Unfortunately, in modern SOI processes, technology scaling has increased the body resistance and body capacitance significantly, limiting body contact effectiveness and adding power dissipation. In spite of this scaling trend, DTMOS still maintains good power-delay and delay performance at low voltages as will be shown in

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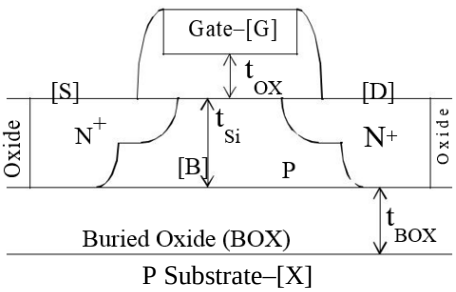
this work. Some PD-SOI characteristics and their affect on DTMOS performance will first be examined and a circuit design style developed to examine DTMOS in its lowest power, highest performance configuration. Simulations in an IBM, 0.13□m PD-SOI technology [6] are then described that compare performance of DTMOS gates to comparable FB-CMOS gates over variations in width, fan-out, fan-in, and wire loading with some extensions made to domino logic. Finally an area comparison is made between the two design styles. The simulations show that DTMOS provides up to 40% reduction in delay with a 20% reduction in power-delay-product over FB-CMOS at 0.5V supply, making DTMOS a good option for low-power design.

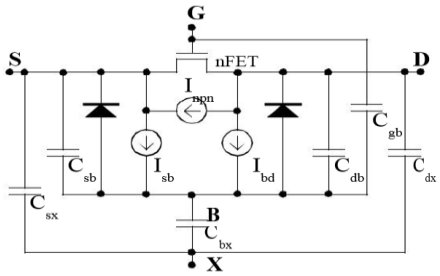
II. SOI TECHNOLOGY

2.1. *SOI Technology Overview*

The main advantage of SOI is its reduced junction capacitance due to oxide isolation of individual circuit elements, resulting in lower-power operation. Additional advantages are good short-channel effects due to shallow source/drain junction depth, latchup immunity, and good soft-error immunity. There are two types of SOI technology, fully-depleted (FD) and partially-depleted (PD). FD-SOI fully depletes the silicon under the channel of charge carriers for the best short-channel behavior in SOI and no floating-body effects; but it suffers from high source/drain resistance and poor processing control of V_T. PD-SOI, shown in Figure 2, has good V_T processing control but does not fully deplete the silicon under the gate of charge carriers, leaving a floating body that affects the performance of the transistor. The floating body causes hysteretic timing patterns, increased subthreshold leakage currents, and the parasitic bipolar effect. The increased subthreshold current occurs due to charge accumulating on the body which lowers V_T. The parasitic bipolar effect occurs when the source, drain, and body are at the same potential and then the source is quickly pulled down, creating a large voltage drop from the body to the source, which forms a base-emitter pair. The parasitic bipolar transistor turns on and conducts current when the device should be off [3]. In spite of these problems, the potential for 20-35% improvement in performance at a given power load over comparable bulk CMOS technology makes SOI the technology of choice for some modern microprocessors [4]-[7].



(a)



(B)

Fig. 2. (a) Schematic cross section of a PD-SOI NFET. (b) Equivalent circuit model. (Inpn is the parasitic lateral npn current, the diodes are the base-emitter and base-collector junction diodes, Isb and Ibd are impact ionization currents.) [3]

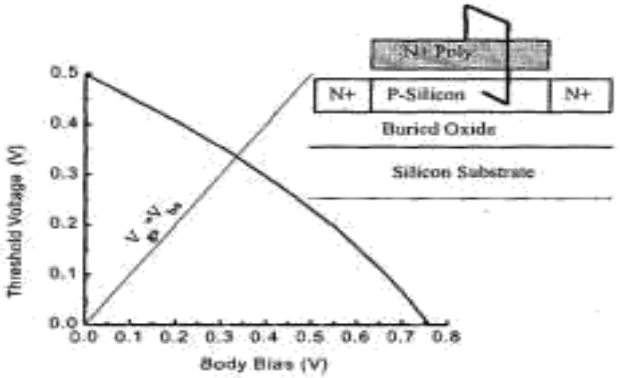


Fig. 3. DTMOS NFET and threshold-voltage variation curve

2.2. SOI design Techniques

All major circuit families can be implemented in SOI. Leakage currents can be offset with weak keepers, level-restoring transistors, or complementary pull-up networks. Floating body effects are mitigated by one or more of the following methods: pre-discharging internal nodes, alternately pre-charging and pre-discharging nodes, re-mapping logic to eliminate large soft nodes, moving parallel transistors closer to ground, and re-arranging or cross-coupling inputs [7][8]. A small margin may also be added to latch hold times or timing requirements may be relaxed. SOI designs can take advantage of current tool sets but there is a disadvantage in that the tools are structured around bulk design techniques which do not leverage SOI's benefits such as increased series stacks [7].

III. DTMOS PERFORMANCE CONSIDERATIONS

Adoption of DTMOS has been limited by the following design challenges: the body capacitance is large and adds power dissipation and gate loading; the body-source and body-drain diodes limit the power supply voltage in order to prevent exponentially growing static currents; the body resistance limits the effectiveness of the body contact due

to the body RC charging delay; the body-drain capacitor has a feed-forward effect that increases gate capacitance; and the body contacts cost a lot of area [7]. The feed-forward effect, extra gate loading, and limited supply voltage are designed around by disconnecting the body from the gate and driving the body from a volt-age source which does not exceed a diode drop, about 0.7V. The area penalty can only be reduced by careful design and will be discussed later. Decreasing the impact of increased gate capacitance, large power dissipation from switching the body capacitance, and body biasing will now be examined in some detail.

3.1. Body Capacitance

Figure 4 shows the body-contacted gate capacitance normalized to the floating-body gate capacitance as the transistor width is increased for single-fingered transistors. The layout of a body-contacted nfet and floating-body nfet of the same width are inset in Figure 2. As can be seen from the layout, the overhead cost of the body contacts results from the T-gate structure and the contact diffusion. The T-gate adds significant gate capacitance, but the amount is fixed so as transistor width increases, the cost penalty of the T-gate decreases. Unfortunately, most logic functions require smaller transistors, so the added loading on the gate impacts DTMOS performance significantly for small gates. Since power and delay are directly influenced by gate-capacitance, they will demonstrate the same exponential decay in their performance as seen in Figure 2.

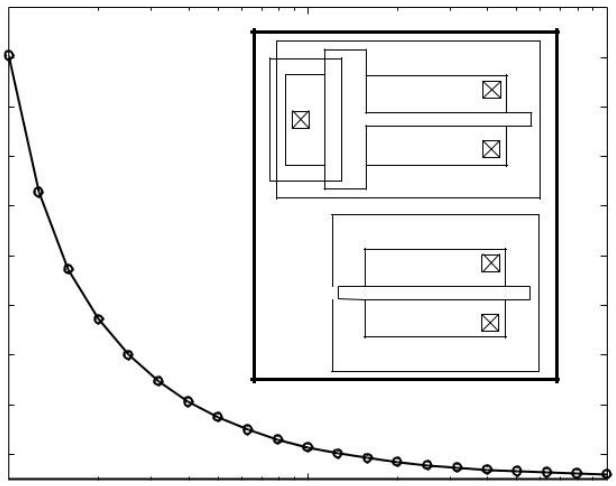


Fig. 4. Body-contacted nfet gate capacitance normalized to floating-body nfet gate capacitance

3.2. Frequency of Switching Body Voltage

Most DTMOS circuits switch the body at the same frequency as the gate. The reason for switching the body with the gate is to limit static power when the transistor is off and increase current when the transistor is switching. The problem with this approach is the added dynamic power that results from switching the body capacitance. The dynamic power dissipation in DTMOS can be approximated by:

$$P_{dyn} = C_L V_{dd}^2 f_L + C_{body} V_{body}^2 f_{body} \quad (1)$$

where C_L is the gate and wire capacitance and C_{body} is the capacitance associated with switching the body. V_{dd} and V_{body} are the load and body supply voltages and f_L and f_{body} are the load and body switching frequencies. In traditional DTMOS, $V_{body}=V_{DD}$ and $F_{body}=F_L$ which means that the power nearly doubles by switching the body since C_{body} is the same order of magnitude as the gate capacitance.

From (1) it is obvious that to reduce power, V_{body} and f_{body} should be reduced since C_{body} is fixed by the circuit design. Some power reduction is obtained from reducing V_{body}, but at least 0.5V is needed for DTMOS to perform better than FB-CMOS as will be described later. With operating voltages in modern technologies around 1V, reducing the supply voltage to 0.5V only reduces the body switching power by 1/4. More power reduction is needed which is obtained by reducing f_{body} to near-static levels compared to f_L.

A body-source bias that is only high when the circuit is on, and then turns off when the circuit is in standby essentially reduces the body-switching power to zero. A near-static body control signal also provides better body control than a fast body control. The body's RC charging time-constant low-pass filters signals that attempt to switch the body too quickly, resulting in a lower body-source voltage than expected. The drawback to using a near-static body control is an increase in static power since the body voltage is always high during circuit operation. Simulations on a DTMOS inverter show that the active power to switch the gate capacitance is 10^3 times the static power for a 0.5V body-source voltage and 10^2 times the static power for 0.6V body-source voltage. Since body capacitance can be as high as gate capacitance, the small increase in static power is at least two orders of orders of magnitude lower than the dynamic power dissipated switching the body at the same frequency as the gate. It should be noted that since the gate capacitance of DTMOS is always higher than FB-CMOS, DTMOS will never dissipate less power than FB-CMOS when both styles are operated at the same frequency and supply voltage.

3.3. Effective body-bias Voltage

Since a near-static bias is the lowest-power configuration for DTMOS, it is important to determine the most effective bias value. Figure 5 charts the delay and static-power dissipation of an FO4 inverter. The static power grows exponentially with body-bias, as expected, but is still two orders of magnitude less than dynamic power at 0.6V body-source voltage. The upper bound of the body-source voltage is limited by static current because at about 0.7V the poor, parasitic bipolar transistor turns on.

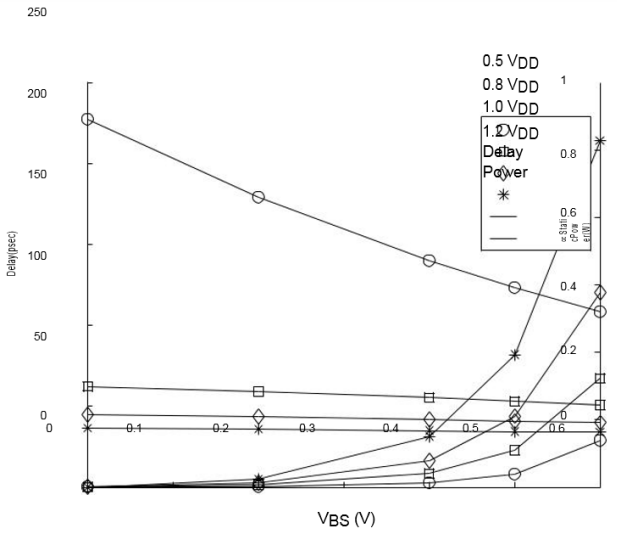


Fig. 5. Static power and delay of FO4 inverter at idths not impacted by body-contact isolation.

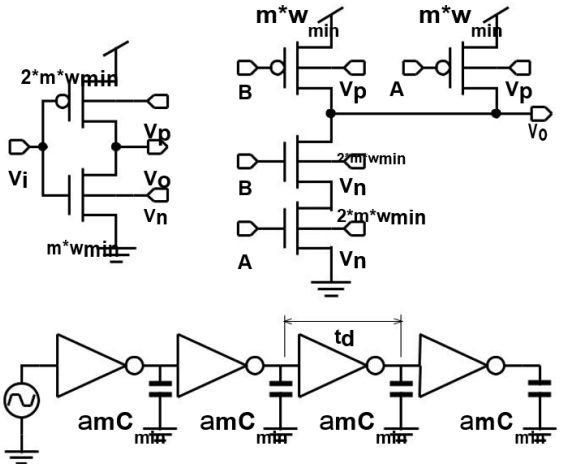


Fig. 6. DTMOS Circuit configurations for simulations. The FB-CMOS gates have the same topology minus the body contacts

IV. Circuit Simulations

The analysis on body-contact show that the lowest-power DTMOS uses a near-static body-bias decoupled from the gate in the range of 0.5V to 0.6V. To character-ize the performance of DTMOS with respect to FB-CMOS, simulations were performed in IBM's 0.13µm PD-SOI technology [6] on the gates in Figure 4. In the figure w_{min} is the nfet minimum width, C_{min} is the input capacitance of a minimum sized inverter, m is the width multiplier, and α determines the wire capacitance. Body conditions are set by static, independent nfet and pfet biases that limit the body-source voltage (V_{BS}) to less than 0.7V. The body-bias inputs are not shown on the inverter chain in Figure 6. Delay and power were measured across the third gate as shown where the gates in the chain were either inverters or NAND gates. Variations in fan-out, device width, V_{DD}, V_{BS}, fan-in, and wire load were simulated to canvass the logic design space. An analysis of the area cost of using DTMOS was also made.

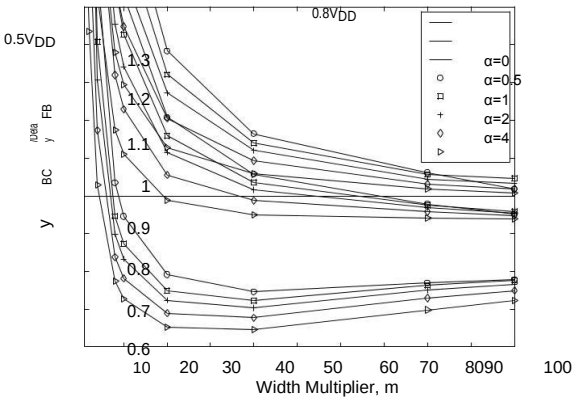
4.1. Fan-Out

Increasing the fan-out increases the loading of the DTMOS inverters and their delay due to the body contact overhead added at each fan-out gate. The added capacitance swamps the increase in drain current for all but low-voltage operation. DTMOS is not faster than FB-CMOS at nominal operating voltages because the FB-CMOS steady-state threshold voltage is higher at high voltages than at low voltages due to impact ionization currents and other body charging mechanisms. Thus, at nominal V_{DD}, the DTMOS current drive is not that much higher than the FB-CMOS and only at very large transistor widths is the added gate capacitance small enough to see a delay improvement in DTMOS.

At low-voltages, DTMOS has a higher threshold volt-age than FB-CMOS and better performance. At 0.5V V_{DD} and 0.5V V_{BS}, delay improves from 10% to 20% over FB-CMOS delay for 50% more power at 20X widths and a 25% delay improvement for widths larger than 40X. The power-delay-product is also lower than FB-CMOS at these widths for a more energy efficient transistor. 20X and larger transistors are reasonable sizes for bus or clock drivers in digital logic but large for inverters in logic functions.

4.2. Wire Loading

Since DTMOS is more suited for driving buses and clock lines an FO1 inverter was simulated over increasing capacitive wire loads. The capacitance of the wire



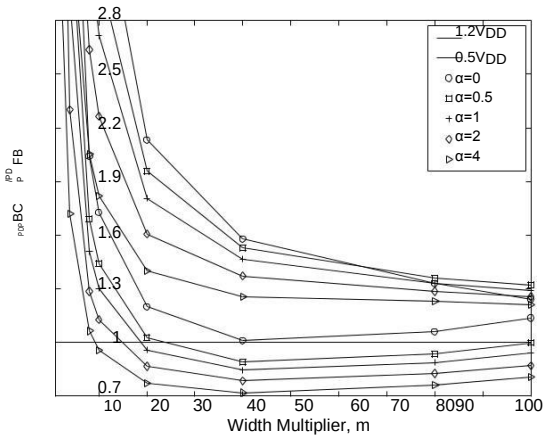


Fig. 7. Normalized FO1 inverter delay and power for various wire loads

load, see Figure 5, is controlled by the parameter α, which is swept from 0 to 4, representing a wire load from 0 to 4 times that of the gate capacitance, mC_{min}. This value is scaled with width so that the wire capacitance is a constant percentage of gate capacitance. Figure 7 shows the simulated normalized delay and PDP of an FO1, DTMOS inverter at V_{BS} = 0.5*V*. Only supply volt-ages of 0.5V and 1.2V are shown in the PDP graph to make it legible.

Normalized delay is reduced by as much as 15% as the wire load, αmC_{min}, of the transistor is increased from 0 to 4 times the inverter input capacitance. Increasing the wire load decreases the overhead of the body contact since more of the gate loading is in the wires. This makes the DTMOS gate more efficient which is why the nor-malized delay and PDP drop as wire loading increases. At 0.8V V_{DD} the normalized DTMOS delay drops to less than one for large gates and high wire loads but the effect is most pronounced at low voltages. At 0.5V V_{DD}, DTMOS delay is 25%-30% lower than FB-CMOS delay and PDP is 14%-21% lower than FB-CMOS for inverters larger than 20X. Gate capacitance is estimated to be between 30% to 50% of the total inverter load with the remaining capacitance coming from wiring and junction capacitance. This corresponds to setting α between 1 and 2. At these wire loads, the DTMOS is faster and more energy efficient than FB-CMOS at low voltages.

4.3. Fan-in

Next to consider is the affect of fan-in on the delay of DTMOS circuits by simulating the NAND gate in Figure 4 with an increasing number of inputs. Since higher fan-in gates are used in logic and will have multiple fan-out, FO4 outputs were simulated to measure the effects of fan-in. Figure 7 shows the normalized delay and PDP of FO4 DTMOS NAND gates with fan-ins of 1, 2, 3, and 4 at V_{BS} = 0.5*V* and α = 0 . The low wire-load was chosen as the worst case for delay and power since it has been shown already that increasing wiring capacitance favors DTMOS by reducing the impact of the body contact on gate input capacitance. The x-axis is the effective pull-down strength of the gate: a NAND2 gate with an effective pull-down width of 2X has nfets with a physical width of 4X. The delay measured is the worst case pull-down delay when the bottom transistor switches last. Adding fan-in adds about the same amount of junction capacitance for DTMOS and FB-CMOS since junction capacitance depends little on the body contact. The added junction capacitance offsets the body-contact capacitance overhead much like wire capacitance does. The large change in normalized delay as fan-in is increased is mostly due to the transistors being much wider to achieved acceptable delay. Even at 1.0V, the high fan-in DTMOS gates are faster than FB-CMOS, but the transistors are large. The DTMOS delay is 20%-40% lower than FB-CMOS delay and the DTMOS PDP is 10%-22% lower than FB-CMOS for FO3 and FO4 gates with effective pull-downs larger than 20X. A large part of the improvement in delay for the higher fan-in gates is due to the physical length of the transistors being large to reduce pull-down delay. This is typical for most logic gates so high fan-in gates have transistors whose sizes may approach the widths at which DTMOS is effective.

4.4. Domino Logic

Domino logic is a popular dynamic logic style used in high-performance VLSI. Domino circuits have a pull-down network driving the input of an inverter. Feed-back from the inverter controls a weak-keeper that prevents leakage and charge sharing in the pull-down from incorrectly evaluating the gate. The simulations performed on fan-out and fan-in can be extended to domino logic in a fairly straightforward manner by adding the pull-down delay of the fan-in to the pull-up delay of an inverter of a similar size and normalizing the sum to a floating-body gate built in the same manner. There are some differences that limit this comparison: the multiple pfets in the NAND gates simulated reduce pull-down time, although the weak keeper in domino gates has this same effect. Since domino gates only drive the nfet pull-down net-work a similar power comparison can't be made. The estimation of domino delay provides a rough measure of how DTMOS will perform in domino logic. Figure 8 shows the estimated domino delay for AND gates com-pose of the FO4 NANDs and the FO4 inverters previously simulated with α=0. This rough estimate shows that domino gates using DTMOS may be faster than FB-CMOS even up to 0.8V V_{DD} for large transistors. Since the transistors in the pre-charge path do not need the extra speed of the body-contact and can be regular floating-body transistors, DTMOS domino can be designed with DTMOS only in the evaluate path, resulting in power savings and area savings.

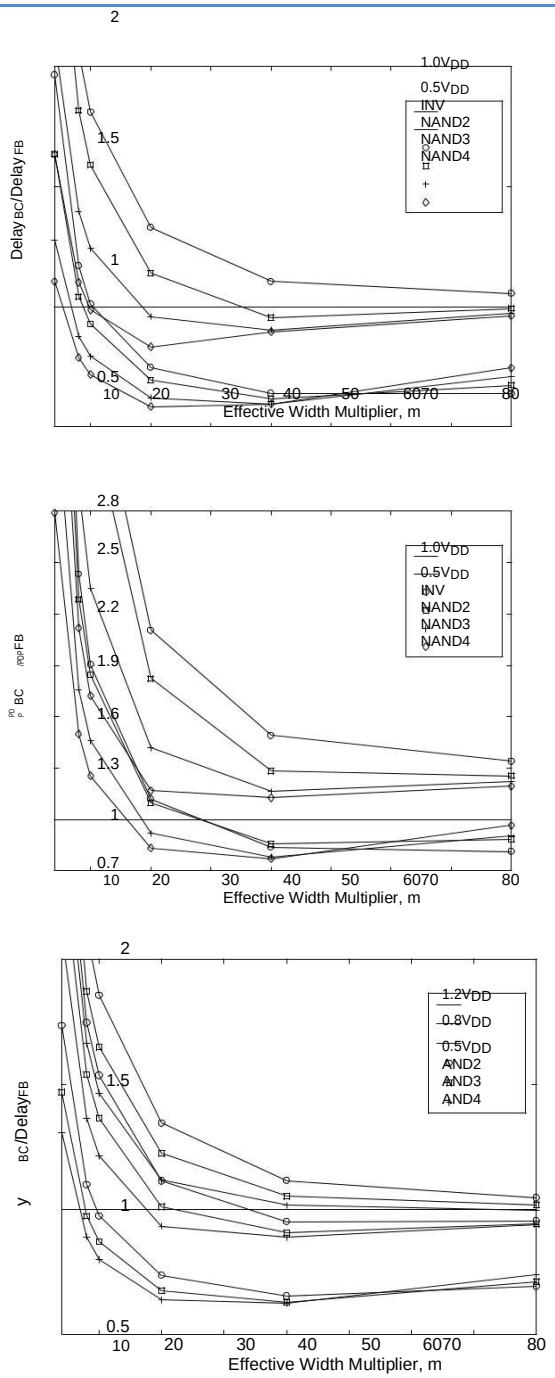


Fig. 8. Width multiplier for different vdd

4.5. Area Penalty

Several DTMOS and FB-CMOS gates with the same netlist were laid out to compare the area of the two logic styles. The DTMOS gates have dual body contacts and external nfet and pfet body-biases. For the domino gates, DTMOS transistors are only used in the input pull-down and output inverter pull-up. The results of the area comparison are shown in Table 1. Small gates such as the

Table 1: Layout area comparison

Gate	*FB(μm^2)*	*DT(μm^2)*
Static 20X inverter	11.8	22.4
Static 20X NAND2	19.4	36
Domino XOR2	17.3	35.9
Domino AND2	12.1	22.4
Domino Booth decoder	146.2	176.3
Domino Booth mux	48.2	97.8
Dual-Rail Domino full-add	86.1	132.1
Domino PGZ gen	58.2	83.7
Domino PGZ merge4	134.7	195.1
Domino PGZ sum	24.8	41.3
24-bit Booth multiplier	57,242	90,441

inverter, NAND, XOR, and AND cover nearly twice the area in DTMOS than in FB-CMOS. The more complex gates range from 1.2 to 2 times larger than FB-CMOS. A 24-bit, floating-point, radix-2 Booth multiplier using all full-adders in the reduction tree would contain roughly 12 decoders, 321 muxes, 260 full-adders, 42 PGZ genera-tors, 105 PGZ merge gates, and 42 PGZ sum gates. This results in a DTMOS multiplier 1.58 times larger than a comparable FB-CMOS multiplier. This is a significant amount of area and represents the main drawback to implementing DTMOS.

Table 2: Normalized delay and power at 0.5V V_{DD}

FO1	α=0, FI1		α=0.5, FI1		α=1, FI1		α=2, FI1	
m	t_d	*PDP*	t_d	*PDP*	t_d	*PDP*	t_d	*PDP*
10	0.95	1.73	0.87	1.44	0.83	1.29	0.78	1.12
20	0.80	1.21	0.75	1.03	0.72	0.95	0.69	0.86
40	0.75	1.01	0.72	0.89	0.70	0.84	0.68	0.79
FO4	FI1, α=0		FI2, α=0		FI3, α=0		FI4, α=0	
m	t_d	*PDP*	t_d	*PDP*	t_d	*PDP*	t_d	*PDP*
10	1.01	1.90	0.93	1.85	0.79	1.45	0.72	1.26
20	0.75	1.13	0.70	1.11	0.62	0.92	0.58	0.83
40	0.64	0.84	0.62	0.86	0.59	0.78	0.60	0.78

around 0.5V provides the lowest-power and lowest-delay. An additional advantage of using near-static DTMOS biasing is the ability to reduce leakage currents during low circuit activity periods by setting the bias to zero volts.

V. CONCLUSION

This study demonstrated that DTMOS is a good circuit design choice for low-power systems targeting sup-ply voltages around 0.5V designed in 0.13µm SOI. The best performance for DTMOS comes when driving large, fixed

wire loads and/or for high fan-in gates. Simulation results show that DTMOS provides reduced delay over FB-CMOS of about 35% for large wire loads and 40% for high fan-in while reducing the energy dissipated by 20% at 20X widths and 0.5V V_{DD}. Table 2 summarizes how delay and PDP change over parameters for FO1 gates and FO4 gates at 0.5V V_{DD}. Of the various topologies of DTMOS available, using a near-static body bias.

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