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New Low Glitch and Low Power Flip-Flop with Gating on Master and Slave Latches

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Abstract **– A new flip flop is presented in which power dissipation is reduced by deactivating the clock signal on both the master and slave latches when there are no data transitions. The new circuit overcomes the clock duty-cycle constraints of previously proposed gated flip-flops. The power consumption of the presented circuit is significantly lower than that of a conventional flip-flop when the D input has a reduced switching activity.**

Keywords **– Flip-Flop, Latches, Master and Slave, Low Glitch, IC Clock.**

I. INTRODUCTION

In recent years the desire for portable computing has steadily grown; the reduction of power dissipation is a crucial factor in IC design. In many applications, the power consumption of the IC clock system is one of the main sources of chip power dissipation. This is due to the high switching activity and the heavy capacitive loading of the clock network. Consequently, many techniques have been recently proposed to reduce clock system power dissipation.

In particular, new flip-flop designs were presented in which the power consumption is reduced due to the clock signal being deactivated (clock gating) when there are no transitions on the D input. Unfortunately, previously proposed clock-gated flip-flops exhibit significant limitations. They require the use of afme-tuned sub-nanosecond pulse generator to be shared among several flip-flops or necessitate having hard constraints imposed on the clock duty-cycle to avoid timing failures.

As the feature size of CMOS technology process shrinks according to Moore's Law, designers are able to integrate more transistors onto the same die. The more transistors there are the more switching and the more power dissipated in the form of heat or radiation. Heat is one of the most important packaging challenges in this era; it is one of the main drivers of low power design methodologies and practices. Another mover of low power research is the reliability of the integrated circuit. More switching implies higher average current is flowing and therefore the probability of reliability issues occurring rises.

The most important prime mover of low power research and design is our convergence to a mobile society. We are moving from desktops to laptops to handhelds and smaller computing systems. With this profound trend continuing, and without a matching trend in battery life expectancy, the more low power issues will have to be addressed. This entails that low power tools and methodologies have to be developed and adhered to. The current trends will eventually mandate low power design automation on a very large scale to match the trends of power consumption of today's integrated chips.

In this paper we present a new flip-flop design in which the gating technique is used for both master and slave latches, overcoming the limitations of previously proposed approaches.

Existed System: The novel conditional-toggle CT_C DET flip-flop design as illustrated in Fig.1. The CT_C flip-flop circuit uses only 20 transistors including transistors for the input, output, and clock buffering. The flip-flop consisting of a dynamic C-element at the output and a latch that provides static behaviour to the circuit. The distinguishing feature of the CT_C flip-flop is the state of its latch doesn't change when the flip-flop's output switches after a clock transition, which leads to low switching energy dissipation.

The circuit for the output of C-element is based but with the feedback inverter eliminated. The inputs to it are input D and the signal that mirrors Q in between clock transitions. As a transistor schematic diagram with consists DET flip-flop of different clock cycles but they are not having any control to the continuation circuit.

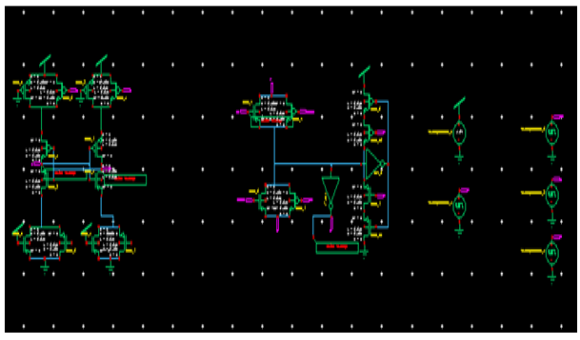

Fig. 1. Schematic of Existed circuit design

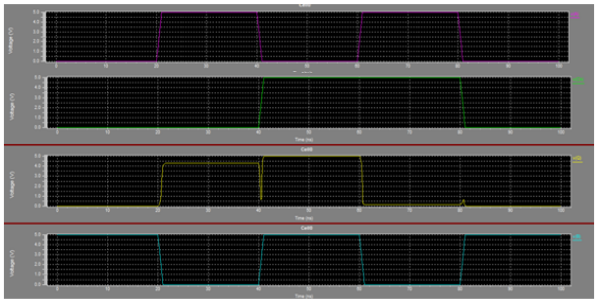

Fig. 2. Simulation wave form of Existed design

Proposed Method: The latch is positive level-sensitive (it is transparent when ckg = 1 and on hold for ckg = 0). The comparison between D and Q is performed by an XOR gate, while the gating logic circuit compromises a simple AND gate. The operation of the circuit is as follows. If ck is 0, then ckg is also 0 and the latch is correctly in the hold state. On the other hand, when ck is high and D is different from Q, the gating logic enables the ckg signal so that the latch can correctly switch. Note that if D is equal to Q the gating logic inhibits the propagation of switching activity from ck to ckg. In this way the power consumption is reduced, assuming that the capacitance on the ckg node is higher than the input capacitance of the gating logic. It is worth noting that the approach shown in Fig. 1 cannot be straightforwardly applied to an edge-triggered flip-flop.

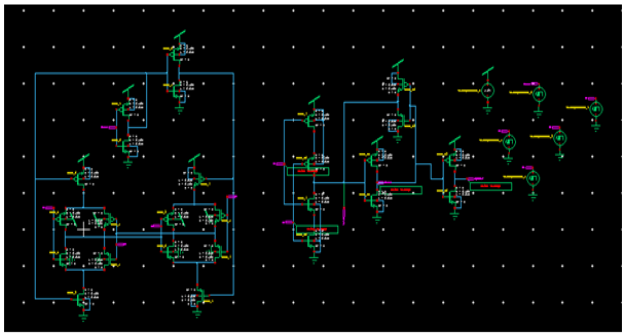

Fig. 3. Schematic of proposed circuit design.

In this case a change of D while ck is high can cause a commutation of ckg, triggering the flip-flop. In previous work this problem has been avoided either by allowing D to change only when ck is low (that is, by imposing a timing constraint on the clock duty-cycle), or by using a fine-tuned sub-nanosecond clock pulse generator. A low-power clock-gated flip-flop that overcomes the limitations of previously proposed approaches can be easily designed by cascading two clock-gated latches in a master-slave configuration. Note that a negative level-sensitive clock-gated latch is quite similar to the schematic circuit diagram shown in Fig. 1, the difference being in the gating logic (implemented with an OR gate) and in the comparator logic (implemented with an XNOR gate). Fig. 2 shows, as an example, the schematic diagram of a clock gated flip-flop in which latches are simple static transmission-gate circuits. The circuit has been designed joining the comparator and the gating logic in a single complex CMOS gate. In this way the number of nodes is reduced, with a further limitation on the power consumption

The flip-flops were implemented in the 25nm CMOS technology. Implementations were optimized for minimum energy-delay product. For the optimization step, the delay metric was the maximum CK-Q delay because it is straightforward to measure. Optimizations were performed by the simulation tool in an automated fashion: The tool varied transistor sizes within the specified bounds and chose the best sizes for each flip-flop after a number of iterations. The search bounds were chosen so that resultant designs would meet recommended design rules most of the time. Weak transistors were allowed to use minimum width rather than the recommended minimum width as it would otherwise result in poor circuit performance. Simulations were performed on schematic designs. Conservative estimates of layout parasitic were included in the simulation models at both the optimization and final simulation stages. These estimates were provided by one of the features of the design kit: The kit can automatically include its own estimation of the RC parasitic interconnect network into schematic simulation models. Parasitic extraction and post layout simulations were also performed on selected designs and were compared to schematic simulations that used automatic estimation of parasitic. Post-layout simulations showed that the kit's estimates for small designs are often conservative and that compact circuits often perform slightly faster in post-layout simulations than in schematic simulations with the automatic parasitic network estimation turned on.

The simulation test bench that is used in this comparison is very similar to the ones used. The Q output of a simulated flip-flop is connected to a load of four symmetric inverters with their n-type transistors sized at minimum recommended width. The generated data and clock signals are connected to the flip-flop's inputs through two inverters.

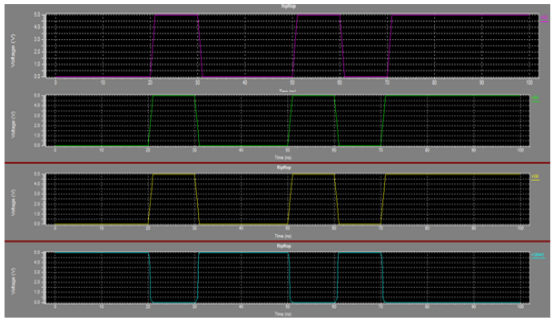

Fig. 4. Proposed circuit wave forms

II. Flip-Flops and Latches

Building a sequential machine that calls for the memory elements which reads a value, saves it for some time and then writes that stored value somewhere else although the element's input value has subsequently changed. A Boolean logic gate can compute values, however it for a while after which writes that stored cost someplace despite the fact that the detail's input value has in the end modified.

Each alternative circuit used as a memory element having its own advantages and disadvantages.

A generic memory element has as internal memory and some circuitry to control access to its internal memory. The memory element which reads its facts from the input

value while advised by the clock and stores that value in its memory. The output displays the saved value, possibly after some delay. In CMOS circuits the memory is formed in two approaches. The primary technique makes uses of positive feedback.

Consequences in a class of elements called multi vibrator circuits.

The second technique to construct memory function in circuits is to use charge storage as a means to store signal values. This technique, which is very famous in MOS world, requires regular refreshing as charge tends to leak away with time.

III. Timing and Delay Definitions for Flip-Flops

The typical overall performance of a flip-flop is qualified through three crucial timings and delays: propagation delay (Clock-to-Output), setup time and preserve time. They reflect within the system level

Overall performance of the flip-flops.

Setup time and keep time outline the connection among the clock and enter data.

Propagation Delay

Propagation delay (Clock-to-Output) is the time delay after arrival of clock's active edge that output is considered as stable.

Clock-to- Output equals the time it takes for the output to change after the occurrence of the clock side. Propagation delay differs for low-excessive transitions and excessive-low transitions.

tClock−to−Output= max(tClock−to−OutputLH, tClock−to−OutputHL)

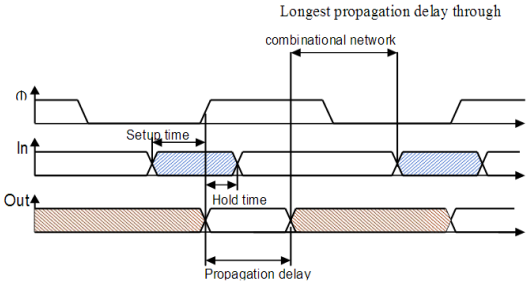

Fig. 5. Timing definitions

Setup Time

To function correctly, the edge-triggered flip-flop requires the input to be stable some time before the clock's active edge.

As setup time may additionally range for low-excessive transitions and excessive-low transitions, setup time is by using definition most of the values obtained for low-excessive and high-low transitions:

tsetup= max (tsetupLH, tsetupHL).

Hold Time

Flip-flop design requires the state of the input to be held for a while after the clock edge. Hold time is by definition most of the values received for low-high and high-low transitions:

Thold= tmax(tholdLH,tholdHL)

The definitions of setup times hold times and propagation delays are illustrated in the timing diagram of above figure in those definitions, propagation delay, setup time and hold time are considered as independent variables. However what hap pens in reality shows that those parameters are not independent from each other, As an example, propagation put off is strongly related with the information arrival time. Propagation put off expands as records arrive later. When data records arrival time could be very close to clock edge, the Clock to Output delay increases drastically.

Comparison Table

Parameter	Existed Method	Proposed Method
Delay	0.5ns	0.21ns
Power	3.97 mw	3.06 mw
Power Delay Product (PDP)	19.85 PJ	6.426 PJ

Conclusion

In this paper a new low-power flip-flop design where in which a gating approach is used for both master and slave latches is presented. The new brand circuit represents an improvement on formerly proposed approaches at the cost of an increased circuit complexity.

The usage of the proposed clock-gated flip-flop results in a significant power saving when the input signal switching activity is low.

From this proposed system to achieve low power and delay. The main aim to calculate the power and delay product (PDP).

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