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Transistor Level Implementation of Vedic Multiplier by using GDI Method

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Abstract **- Low power design has significant importance in digital VLSI circuits. Speed and power efficient implementations of multipliers are very challenging. The increase in complexity of VLSI systems and minimizing power consumption has clearly become a priority. The processor performance depends upon the power and delay, as we get less the effective processor. The proposed paper consists of the transistor level implementation of vedic multiplier using Urdhva Tiryakbhyam (uv) sutra. This low power vedic multiplier designed by using the GDI-MUX technique. So, these GDI based design of multipliers may reduce power consumption compared to that of design in CMOS. These low power designs are realized in MICROWIND TOOL schematic tool.**

Keywords **- Vedic Multiplier, Urdhva Tiryakbhyam, Gate Diffusion Input.**

I. INTRODUCTION

Vedic Mathematics has been introduced by Jagadguru Swami Sri Bharathi Krishna Trithaji Maharaja known to us by the name of scholar in Mathematics. He made the research on mathematics relating to the sixteen sutras and thirteen sub sutras. Vedic multiplication generally includes the effective algorithms for using in various engineering applications for computing purposes. Vedic multiplication consists of natural principles to toggle between how the human brain is working. Comparing to conventional mathematics, vedic mathematics have only less number of manipulation steps for high speed arithmetic operation. Ancient vedic multiplication has totally sixteen sutras followed by thirteen sub sutras, in very popularly used two sutras are Urdhva Triyakbhyam sutra and Nikhilam Sutra. Vedic multiplication has been widely used in the mathematics circle extending to the geometry and cosine, sine, tan functions.

It becomes popular due to its applications via through the simple applicability logical operations and uniformity in arrangement. Nowadays research have been made in India and in abroad by scholars because of its ability to make the calculation eminent for easy understanding. Considering the power consumption of a multiplier, lot of works related to research has been carried out for years. The multiplier cell [1] has been constructed using the pass transistors and there by using the n-pass transistors as cross coupled devices to reduce the delay of the multiplier circuit. The speed and overall performance of Vedic multiplier [2] is calculated by various low power multiplier architectures and comparison is made for it to analysis the power consumption. A design of 4 bit Vedic multiplier design using transistors at the gate level analysis of for maximum power reduction yields [3]. This proposed paper has the 8 bit Vedic multiplier structure is built using the partial product row using AND gate, which is followed by the carry save adder block consisting of full adder and AND gate, which is again followed by the carry propagate adder block consists of chain of full adders in parallel fashion. Finally we got the partial products for the 8bit Vedic multiplier, as the 16 bit partial product output is arrived using Vedic multiplication technique. The AND gate used in this paper is built using GDI logic which is used for generating partial products instead of 5T AND gate design or conventional method. The full adders used in the proposed Vedic multiplier design uses the 6T PTL logic which is having the prominent feature of using transistor count to the least extent and less power consumption compared to the conventional 28T full adders. The remaining paper is consisting of following sections as, Section II provides the Architecture of Urdhva Tiryakbhyam Sutra techniques for multiplying the 8 bit number using Vedic multiplication. Section III provides the Multiplier blocks which carries the AND gate structure, half adder structure, full adder structure. Section IV comprises of Multiplier architectures for 2 bit, 4 bit and proposed 8 bit using 6T PTL full adders. Section V concludes the paper with power estimation and future work.

II. ARCHITECTURE OF URDHVA TIRYAKBHYAM SUTRA

The fast multiplication operation has been carried out by ancient Vedic mathematical approaches for parallel computing of partial products of Vedic multiplier to reduce the power and delay. Urdhva Tiryakbhyam Sutra is an effective algorithm for effective computing of two or more numbers. This Sutra technically means that vertically and cross wise, which is a two digit decimal multiplication. The conventional method of multiplication is hard with many limitations and computational steps are larger so we use Vedic multiplication for more power efficient output and quick

as less number of steps. Generally the Vedic multiplication requires the multiplicand and multiplier to form the partial products in the way of as indicated by the UT Sutra as vertically and cross wise lines are figured using AND gate.

III. MULTIPLIER BLOCKS

The UT Sutra of Vedic mathematics is used to built the proposed 8 bit multiplier architecture. The overall proposed Vedic multiplier design uses the 2T AND gate design and uses the 6T PTL full adders, which ensures the overall significant reduction on chip area which is accumulated by the multiplier. Drastically as the number of transistor count for the AND gate, half adder, full adder topology is reduced to optimise the overall power consumption of the Vedic multiplier. The proposed Vedic multiplier has the low power, high speed and full swing operations based on the attributes of the related multiplier characteristics for maximum power reduction. As the multiplier block mainly consist of adder chains and AND gate chains. The chain of AND gate is used to generate or carry out the partial product of multiplier. The chain of adders is used to summand those AND gate blocks. In conventional multiplier the latency increases due to the long adder tree structures which is the limitation for speed.

A. Basic GDI Cell

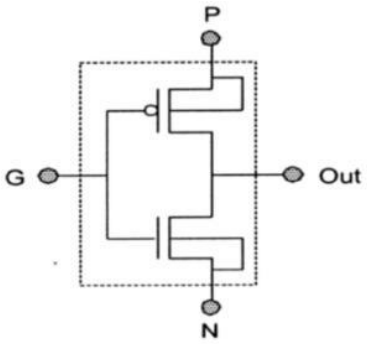

Fig. Basic GDI Cell

N	P	G	OUT	FUNCTION
'0'	B	A	A'B	F1
B	'1'	A	A'+B	F2
'1'	B	A	A+B	OR
B	'0'	A	AB	AND
C	B	A	A'B+AC	MUX
'0'	'1'	A	A'	NOT

Table: Various Logic Functions of GDI cell

B. AND Gate

A 2T based AND gate design is carried out in the proposed Vedic multiplier for partial product generation in the first row of the carry save arrangement. AND gate is designed using GDI or Gate Diffusion Input technique because of low power construction as it requires only two transistors for designing the AND structures. The new 2T AND gate GDI logic structures provides the multiplier with partial products of least delay.

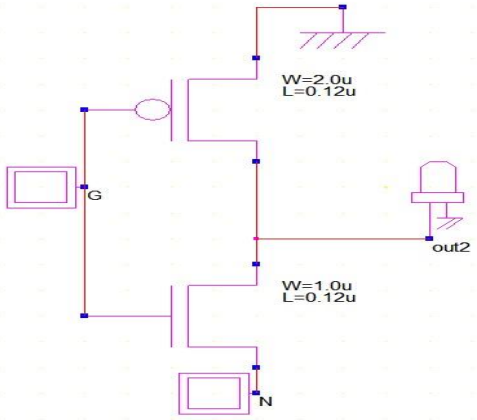

Fig. GDI AND gate

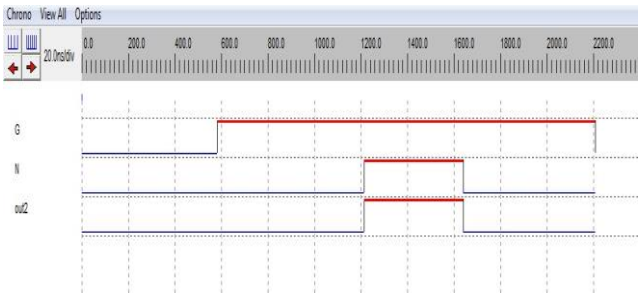

Fig. Output Waveform of AND gate

C. Half ADDER

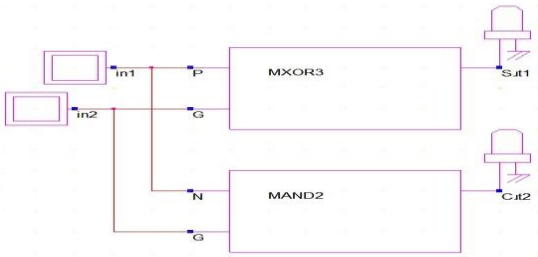

Fig. GDI Half Adder

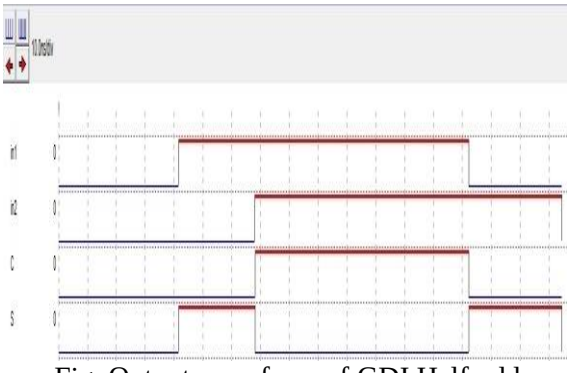

Fig. Output waveform of GDI Half adder

D. *Full ADDER*

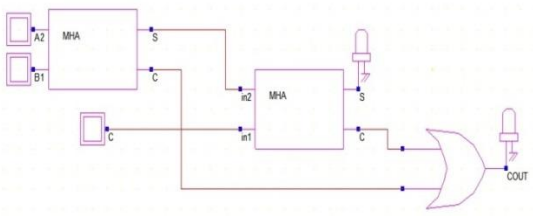

Fig. 5. GDI Full Adder

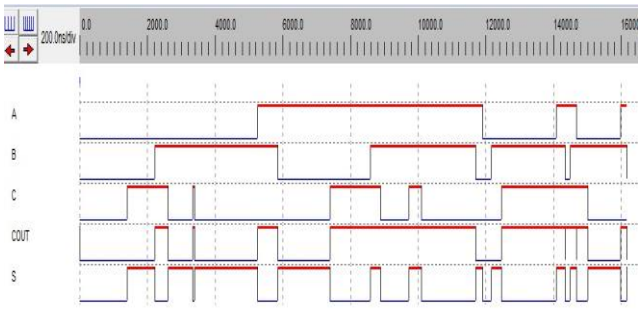

Fig. Output waveform of GDI FA

IV. MULTIPLIER ARCHITECTURE

A.2. BIT Vedicmultiplier Architecture

The 2-bit Vedic Multiplier Architecture is built using four AND gates and two half adder structures based on UT Sutra. The design is followed by the multiplication of two bit numbers of aO, al, bO and bl. The two bit vedic multiplication gives the partial products pO, pl, p2 and p3 as output. Here the addition operation is carried out by two half adders and multiplication is carried out by the chain of AND gates.. This parallel computation of partial products yield the high speed adder structure and the overall multiplier performance is significantly improved, and delay is reduced.

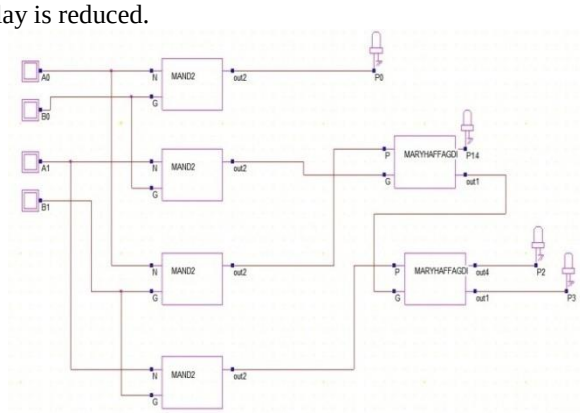

Fig. GDI 2-Bit Vedic multiplier

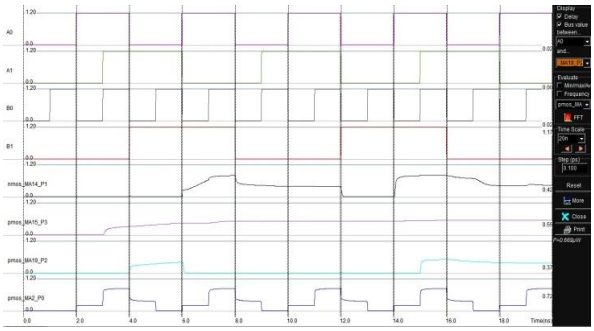

Fig. Output Waveform of GDI 2-Bit Vedic multiplier

B. 4-BIT Vedic Multiplier Architecture

The 4-bit Vedic Multiplier Architecture is built using the four 2-bit Vedic Multiplier, two 4 bit carry save adders and a 4 bit ripple carry adder. Now the carry save arrangements consist of chain of full adders which there by sub linked to the ripple carry adder arrangements. The design is followed by the multiplication of two bit numbers of aO, al, a2, a3, bO, bl,b2 and b3 using UT Sutra. This carry save arrangements consist of full adders and half adders in the first bit addition stage and finally merged with ripple carry arrangement of full adders there by the carry out is linked with carry in. The partial product addition is completed by the carry save adder arrangements and final ripple carry adder, so that to the proposed work in the multiplication task. In terms of compactness of the multiplier design for drastic improvement of power and delay. We use AND gate for partial product generation and adder blocks for summing operation to produce the final output of partial products of pO, pl,p2, p3,p4, p5,p6 and p7. Totally power reduced to the most in this carry save arrangements for the 4 bit vedic structure.

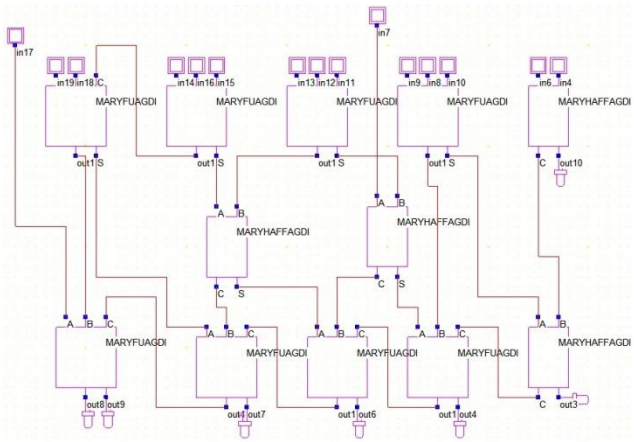

Fig. GDI 4-Bit Vedic multiplier

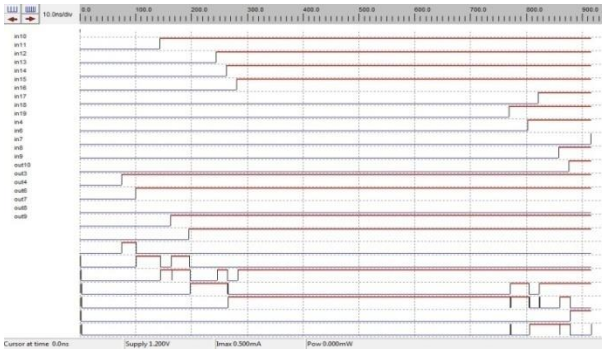

Fig. Output Waveform of GDI 4-Bit Vedic multiplier

V. RESULT

Table 7.1: Comparison between the existed and proposed design

PARAMETER	EXISTED SYSTEM			PROPOSED SYSTEM
	CMOS FA	TG FA	TG PSUEDO FA	GDI
AREA (µm2)	544	280	273	98
POWER DISSIPATION (µw)	45.35	33.56	19.33	3.16
NO.OF TRANSISTORS	28	16	19	14
DELAY(ns)	1.76	4.28	1.15	0.6

VI. CONCLUSION

The proposed design compare with the another full adder techniques the power dissipation and delay are more. The speed of the circuit less. By using GDI full adder technique designing a most efficient 2-bit, 4-bit vedic multiplier. The number of transistors will be less because of these reason it occupies less area and high speed.

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