

Design of Low Power Double Tail Comparator using CMOS Technology

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Abstract – The need for low-power, area efficient and high speed analog-to-digital converters is pushing toward the use of proposed dynamic double tail comparator to maximize speed and power efficiency. In this paper, the layout of proposed double tail comparator is designed using Microwind3.1 version and compiled for desired results. In DSCH3.1 version the Schematic of proposed comparator is runned. From these designers can obtain an intuition about the main contributors to the comparator delay and fully explore the tradeoffs in dynamic comparator design. Based on the presented analysis, a new dynamic comparator is proposed, where the circuit of a conventional double tail comparator is modified for low-power and fast operation even in small supply voltages. Without complicating the design and by adding few transistors, the positive feedback during the regeneration is strengthened, which results in remarkably reduced delay time. Post-layout simulation results in a 90nm CMOS technology confirm the analysis results. It is shown that in the proposed dynamic comparator both the power consumption and delay time are significantly reduced.

Keywords – Analog-to-digital Converters, Proposed Double Tail Comparator.

I. INTRODUCTION

Apart from technological modifications, one of the most important analog circuits required in many analog integrated circuits is comparator. It is used for the comparison between two same or different electrical signals. The Comparator design becomes an important issue when design technology is scaled down. Due to the non-linear behaviour of threshold voltage (V_t) when design technology is scaled down, performance of Comparator is most affected. Many versions of comparator are proposed to achieve desirable output in sub-micron and deep sub-micron design technologies. The selection of particular topology is dependent upon the requirements and applications of the design. Low power circuit design has emerged as a principal theme in today's electronics industry. In this project comparator architecture their design parameter, study about offset voltage and sources of power and their estimation and reduction technique are discussed. Developing new circuit structures which avoid stacking too many transistors between the supply rails is preferable for low-voltage operation, especially if they do not increase the circuit complexity. In additional circuitry is added to the conventional dynamic comparator to enhance the comparator speed in low supply voltage. This circuit is our required double tail comparator which is designed to avoid stacking, complexity, rail to rail is low voltage preferable and reaches the desirable results using 90nm CMOS technology.

The designing high-speed comparators is more challenging when the supply voltage is smaller. In other words, in a given technology, to achieve high speed, larger transistors are required to compensate the reduction of supply voltage, which also means that more die area and power is needed. Besides, low-voltage operation results in limited common-mode input range, which is important in many high-speed ADC architectures, such as flash ADCs. Many techniques, such as supply boosting methods techniques employing body-driven transistors current-mode design and those using dual-oxide processes, which can handle higher supply voltages have been developed to meet the low-voltage design challenges. Boosting and boot strapping are two techniques based on augmenting the supply, reference, or clock voltage to address input-range and switching problems. These are effective techniques, but they introduce reliability issues especially in UDSMCMOS technologies. Body-driven technique adopted by Blalock removes the threshold voltage requirement such that body-driven MOSFET operates as a depletion-type device.

In electronics, Operational amplifier (Op-amp) is designed to be used with negative feedback. It can be also used as comparator in open loop configuration. On the other hand, comparator is especially designed for open loop configuration without any feedback. Hence it is the second most widely used device in electronic circuits after Op-amp. Comparators are known as 1-bit analog-to-digital converter and for that reason they are mostly used in large abundance in A/D converter. In the analog-to-digital conversion process, it is necessary to first sample the input. This sampled signal is then applied to a combination of comparators to determine the digital equivalent of the analog signal. The conversion speed of comparator is limited by the decision making response time of the comparator. Apart from that, comparators are also can be found in many other applications like zero-crossing detectors, peak detectors, switching power regulators, data transmission, and others. The basic functionality of a CMOS comparator is used to find out whether a signal is greater or smaller than zero or to compare an input signal with a reference signal and outputs a binary signal based on comparison.

CMOS evolution has come to a point where for analog circuits new phenomena need to be taken into account. A major issue is the decreasing supply voltage. Although the supply voltage has dropped from 5V in the early nineties down to 1.2V today, most analog circuits can still be designed. However, a further drop in supply voltages is expected to cause serious road blocks for analog circuits, because the signal head room becomes too small to design circuits with sufficient signal integrity at reasonable power

consumption levels. Although the analog transistor properties do not really get worse when comparing the mat identical bias conditions, lower supply voltages require biasing at lower operating voltages which results in worse transistor properties, and hence yield circuits with lower performance. These cond issue is gate leakage. Gate leakage will increase drastically when migrating to newer technologies. When the gate oxide thickness is reduced with the equivalent of one atomic layer, the gate current increases by approximately one order of magnitude. Despite technological remedies, gate leakage will become part of analog design-especially for long transistors. In this paper a new dynamic comparator is presented, which does not require boosted voltage or stacking of too many transistors. Merely by adding a few minimum-size transistors to the conventional double- tail dynamic comparator, latch delay time is profoundly reduced. This modification also results in considerable power savings when compared to the conventional dynamic comparator and double tail comparator.

II. DOUBLE TAIL COMPARATOR

Comparator is one of the fundamental building blocks in most analog-to-digital converters (ADCs). Many high speed ADCs, such as flash ADCs, require high-speed, low power comparators with small chip area. High-speed comparators in ultra deep sub micrometer (UDSM) CMOS technologies suffer from low supply voltages especially when considering the fact that threshold voltages of the devices have not been scaled at the same pace as the supply voltages of the modern CMOS processes.

A. Proposed Double-Tail Dynamic Comparator

The following Fig.I demonstrates the schematic diagram of the proposed dynamic double tail comparator. Due to the better performance of double-tail architecture in low-voltage applications, the proposed comparator is designed based on the double-tail structure. The main idea of the proposed comparator is to increase $\Delta V_{fn/fp}$ in order to increase the latch regeneration speed. For this purpose, two control transistors (M_{c1} and M_{c2}) have been added to the first stage in parallel to M_3/M_4 transistors but in a cross-coupled manner.

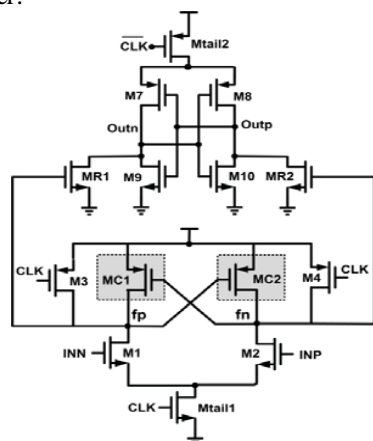


Fig. I. Schematic diagram of the proposed Double Tail Comparator [Main idea]

B. Operation

The operation of the proposed comparator is as follows. During reset phase ($CLK=0$, M_{tail1} and M_{tail2} are off, avoiding static power), M_3 and M_4 pulls both fn and fp nodes to VDD , hence transistor M_{c1} and M_{c2} are cut off. Intermediate stage transistors, MR_1 and MR_2 , reset both latch outputs to ground. During decision-making phase ($CLK=VDD$, M_{tail1} , and M_{tail2} are on), transistors M_3 and M_4 turn off. Furthermore, at the beginning of this phase, the control transistors are still off (since fn and fp are about VDD). Thus, fn and fp start to drop with different rates according to the input voltages. Suppose $V_{INP} > V_{INN}$, thus fn drops faster than fp , (since M_2 provides more current than M_1). As long as fn continues falling, the corresponding pMOS control transistor (M_{c1} in this case) starts to turn on, pulling fp node back to the VDD ; so another control transistor (M_{c2}) remains off, allowing fn to be discharged completely. In other words, unlike conventional double-tail dynamic comparator, in which $V_{fn/fp}$ is just a function of input transistor trans conductance and input voltage difference, in the proposed structure as soon as the comparator detects that for instance node fn discharges faster, a pMOS transistor (M_{c1}) turns on, pulling the other node fp back to the VDD . Therefore by the time passing, the difference between fn and fp ($\Delta V_{fn/fp}$) increases in an exponential manner, leading to the reduction of latch regeneration time.

Despite the effectiveness of the proposed idea, one of the points which should be considered is that in this circuit, when one of the control transistors (e.g., M_{c1}) turns on, a current from VDD is drawn to the ground via input and tail transistor (e.g., M_{c1} , M_1 and M_{tail1}), resulting in static power consumption. To overcome this issue, two nMOS switches are used below the input transistors [M_{sw1} and M_{sw2}], as shown in Fig. 2.

At the beginning of the decision making phase, due to the fact that both fn and fp nodes have been pre-charged to VDD (during the reset phase), both switches are closed and fn and fp start to drop with different discharging rates. As soon as the comparator detects that one of the fn or fp nodes is discharging faster, control transistors will act in a way to increase their voltage difference. Suppose that fp is pulling up to the VDD and fn should be discharged completely, hence the switch in the charging path of fp will be opened, but the other switch connected to fn will be closed to allow the complete discharge of fn node. In other words, the operation of the control transistors with the switches emulates the operation of the latch.

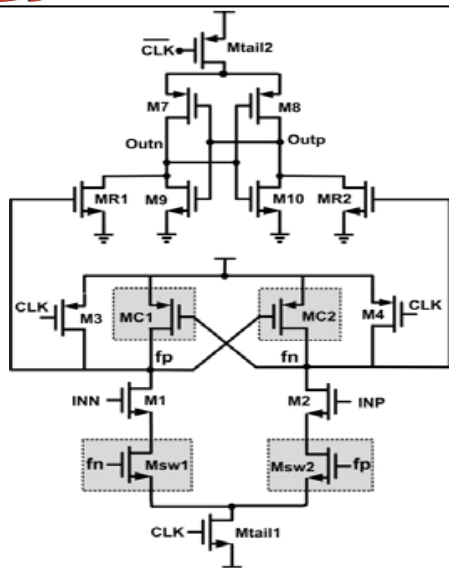


Fig II. Schematic diagram of the proposed Double Tail Comparator [Final structure]

Therefore by the time passing, the difference between f_n and $f_p V_{f_n}/f_p$ increases in an exponential manner, leading to the reduction of latch regeneration time. Despite the effectiveness of the proposed idea, one of the points which should be considered is that in this circuit, when one of the control transistors (e.g., Mc1) turns on, a current from VDD is drawn to the ground via input and tail transistor (e.g., Mc1, M1, and Mtail1), resulting in static power consumption. To overcome this issue, two NMOS switches are used below the input transistors.

III. SIMULATION

Initially we are going to open digital schematic 3.1 software. Double click on DSCH3.1 software than automatically opens a new window. Right side of the window it have a design component tool slide is present there. By using those design parameters we are going to draw our schematic as our requirement.

A. Schematic

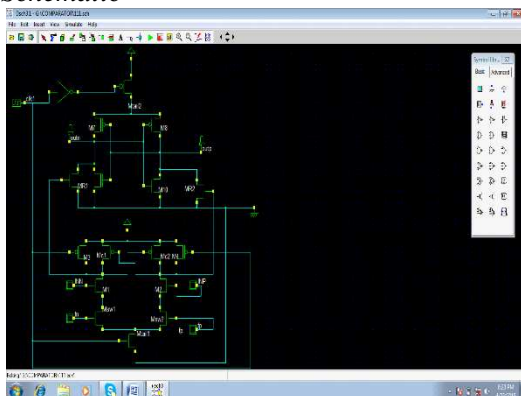


Fig. III. Schematic

Finally we draw the digital schematic according to our project. Now we are going to give the code for our schematic. But in Digital Schematic 3.5 software here

itself have the capability to generate the code according to our schematic

B. Verilog Code

After drawing the schematic. Than we go to file and it have an option make verilog file, we are click the verilog file making icon than it generate the verilog code for our digital schematic later we click on ok button it generates the code as shown below.

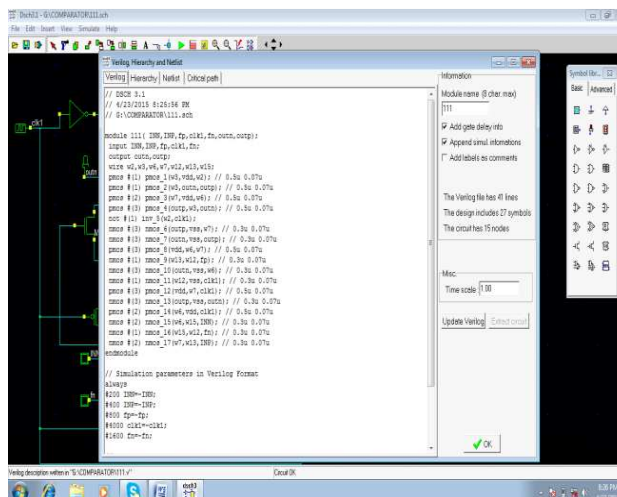


Fig. IV. Verilog file generation

C. Compilation of Verilog File

Now we are going to compile that verilog file by using Micro Wind 3.5 software. The verilog code in the above fig. is written for Double-Tail comparator. In this as we change the supply voltages and clock signals the power value also changes. The power consumption decreases for Double-Tail comparator as compared to Conventional Dynamic comparator.

In this project the off-set voltages of a Double-Tail comparator decrease as in turn power consumption also decreases as compared to Conventional Dynamic comparator.

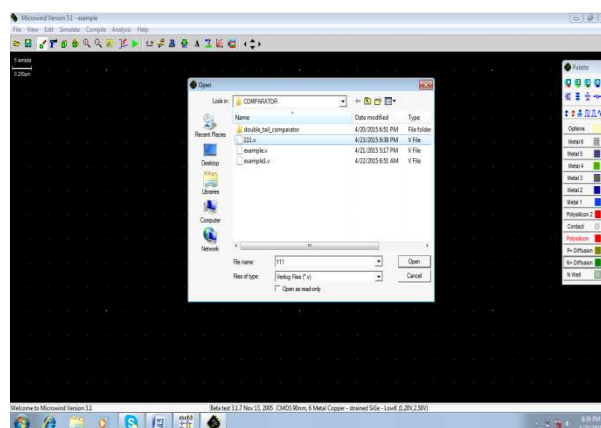


Fig. V. Compilation of verilog file

First of all we are double click on Micro Wind software than automatically it creates a new window. Here we able to see a COMPILATION option at the top of the taskbar by using these compilation button it have an another two

options, compile verilog file is one of that. By using the COMPIL E VERILOG FILE we are going to open our verilog code in the Micro Wind software. Then it compile the verilog code for our schematic.

D. Verilog File Compilation

It compile the verilog code in Micro Wind software it generates the new window. Here we are going to click on COMPIL button. After compilation came back by using BACK TO EDITOR button.

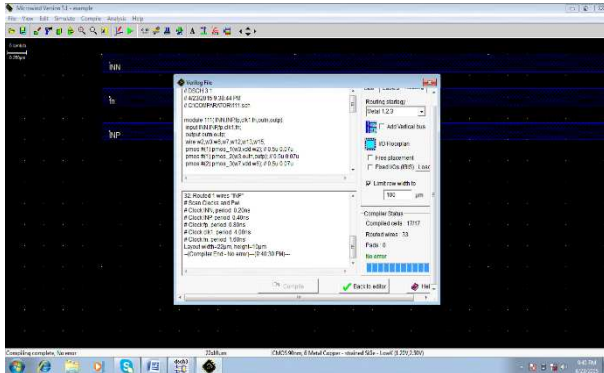


Fig. VI. Compilation of verilog code in Micro wind

After coming back to the editor it generates the LAYOUT for our schematic

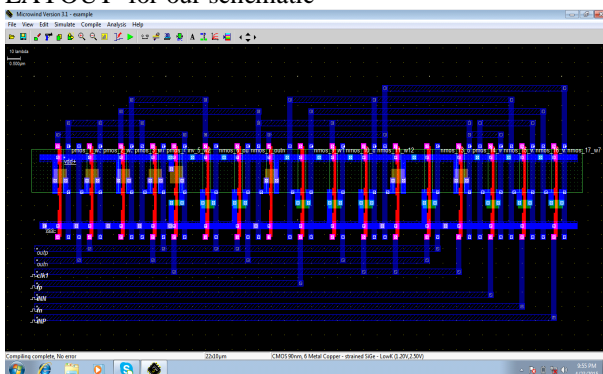


Fig. VII. Layout for Double Tail Comparator

IV. SIMULATED WAVEFORMS

A. Voltage Versus Time

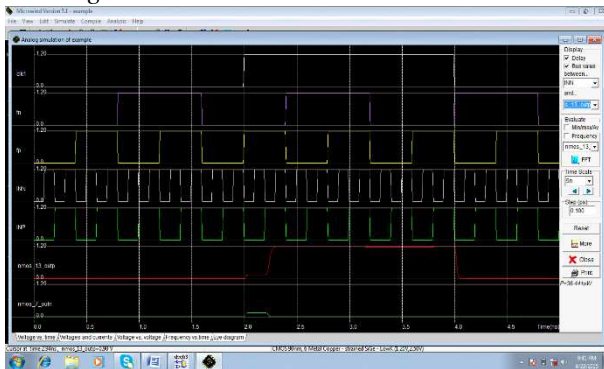


Fig. VIII. Voltage versus time wave form

B. Voltage Versus Current



Fig. IX. Voltage versus current wave form

C. Voltage Versus Voltage

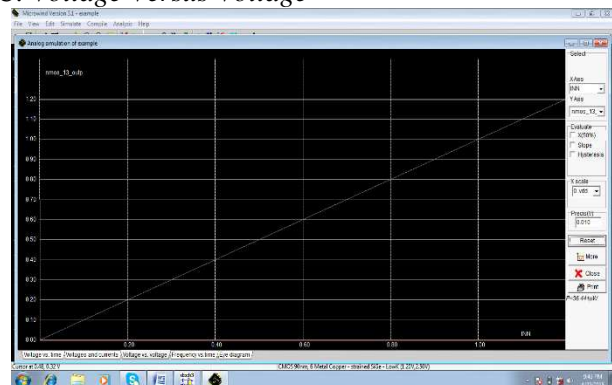


Fig. X. Voltage versus voltage wave form

D. Frequency Versus Time



Fig. XI. Frequency versus time wave form

E. Eye Diagram

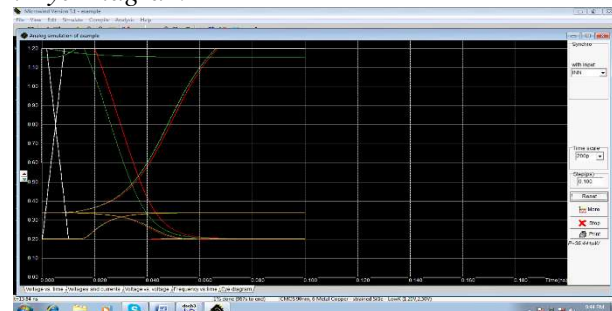


Fig XII: Eye diagram

V. CONCLUSION

Two common structures of conventional dynamic comparator and conventional double-tail dynamic comparators were analyzed. Also, based on theoretical analyses, a new dynamic comparator with low-voltage low-power capability was proposed in order to improve the performance of the comparator. Post-layout simulation results in 90nm CMOS technology confirmed that the delay of the proposed comparator is reduced to a great extent in comparison with the conventional dynamic comparator and double-tail comparator. The stacking, complexity, power consumption are reduced when compared to the conventional dynamic comparator.

VI. ACKNOWLEDGMENT

As mentioned earlier, since the proposed double tail dynamic comparator can be optimized for either the minimum offset voltage or the maximum load drivability at a limited area according to the design specification, searching for the most suitable application can be one topic for the future works. In addition, offset cancellation techniques can be considered for further reduction of the offset voltage.

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