International Journal of Engineering Innovation & Research
Volume 6, Issue 1, ISSN: 2277 – 5668

Area Optimized Adder Design Using Carry Selection Logic in Power-Constrained Environments

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Date of publication (dd/mm/yyyy): 25/02/2017

Abstract **– The major drawback of the parallel adder is its slow speed due to the time it takes to propagate the carry. Also in parallel adder the delay increases linearly with the bit length. To overcome this limitation some papers work on carry look ahead adder but on the area draw back. But CLA requires large number of transistor for design with increase area. The main purpose of this paper is to design the speed limiting and area efficient adder design with optimize power. For speed limitation the carry select technique if use and for optimized power and reduced area. The design logic has been design using 50nm technology on Micro wind layout simulator. Compared to a conventional adder with this architecture, The layout design by dynamic CMOS logic optimizes the area in term of number of transistors with the comparison of conventional adder logic.**

Keywords **– Area, Speed, power, Transmission Gate, Carry Select.**

I. INTRODUCTION

Addition is the most common and often used arithmetic operation on microprocessor, digital signal processor, especially digital computers. Also, it serves as a building block for synthesis all other arithmetic operations. Ripple-carry, Carry-select and Carry-look ahead to emphasize the common performance properties belong to their classes. There is a slow ripple-carry adder with the smallest area, the carry-skip, carry-select adders with multiple levels have small area requirements and shortened computation times, the carry-look ahead adder and the parallel prefix adder represents the fastest addition schemes with the largest area complexities. For the optimization of speed in adders, the most important factor is carry generation. For the implementation of a fast adder, the generated carry should be driven to the output as fast as possible, thereby reducing the worst path delay which determines the ultimate speed of the digital structure. In the optimization for area, care should be taken in the design of the building blocks of the structure, which determine the area occupied by the architecture and, finally, also affect the speed.

In literature survey there is many High-speed adder architectures available such as carry look-ahead (CLA) adders, carry-skip adders (CSA), carry-select adders (CSA), conditional sum adders , and structural combinations of these adders. Also mostly use adder for its feature of less area is a serial adder. For the power optimization purpose adder is design using transmission gate. As transmission gate base design requires few transistors and it avoids the stray capacitances which reduce the power consumption.

In this paper a transmission gate base logic is design using 50nm CMOS technology. A cascaded structure is design for multiple bit add ion logic. The size of CMOS transistors is changes with the change of channel length and channel width (W/L) ratio. It also depends on the parasitic resistances and capacitances. Use of transmission gate in design reduces the size of transistor. The basic structure of transmission gate base logic constitutes of multiplexer logic.

II. RELATED WORK

Manish Kumar Jaiswal, Ray C. C. Cheung, propose an architecture of a double precision (DP) adder, which also supports a dual (two parallel) single precision (SP) computational feature. Its architecture, includes comparator, swap, dynamic shifters, leading one-detector (LOD), mantissa adders/subtractors, and rounding circuit, The proposed architecture has been synthesized for OSUcells Cell 0.18 μm technology ASIC implementation. Compared to a standalone DP adder with two SP adders, the proposed unified architecture can reduce the hardware resources by ≈ 35%, with a minor delay overhead [1]. Zaher Owda, Costas Efstathiou design carry look ahead adder on 90nm technology using machester carry chain adder logic. A 8 bit CLA is design using two independent 4-bit carry chains. Ali K. Horestani design the high speed full adder with optimize area on 0.18μm CMOS technology with 1.8v power supply. This work gets the propogation delay of 2.02ns with 7.8% of speed improvement. The design can be implemented with 10% reduction in number of transistors with 2.1% of power reduction [2]. Basant Kumar Mohanty and Sujit Kumar Patel design carry select adder (CSLA) is an RCA–RCA (ripple carry adder) configuration that generates a pair of sum words and output carry bits corresponding the anticipated input- carry (cin = a 0 and 1) and selects one out of each pair for final-sum and final-output-carry This paper work on the carry select (CS) operation which is scheduled before the calculation of final-sum, which is different from the conventional approach. Bit patterns of two anticipating carry words (corresponding to cin = 0 and 1) and fixed cin bits are used for logic optimization of CS and generation units with less area and delay than the recently proposed BEC-based CSLA. Their synthesis result shows that the existing BEC-based Square root carry select adder (SQRT-CSLA) design involves 48% more area delay product (ADP) and consumes 50% more energy than the proposed SQRTCSLA, on average, for different bit-widths [3].

Speed Trade off due to Carry Propagation

The speed limitation of parallel adder due to the path delay of carry propagation and area trade off is the well known problem. The basic logic cells design by transmission gate is area optimized. As the XOR logic gate

design using CMOS logic requires about 22 transistor whereas the XOR gate design using transmission gate requires about 8 transistors. It also avoids the formation of stray capacitances which is the base power and area optimization. In parallel adder , all full adders are cascaded. Thus every succeeding adder has to wait for the carry out of the previous full adder output carry. The basic building blocks in this adder is the PG generator, carry generator and sum generator.

III. Adder Design with Bypass Logic

To be able to understand 1-bit full adder (FA) cell we have to introduce the most basic addition block that is used as its main constituent, the half adder. The half adder has only two 1-bit inputs, A and B, who's Sum can be calculated by a simple XOR (denoted H) operation. The Sum output is sufficient to express the sum of two 1-bit numbers for three, out of four possible, inputs. The Sum of A=1 and B=1 cannot be expressed by a single bit, and a result with a higher significance than the Sum is required.

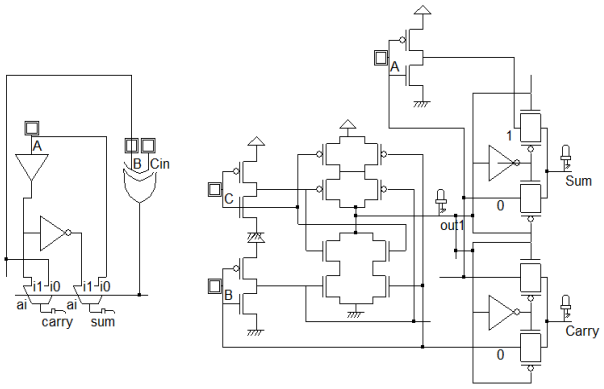

Fig Full Adder design using bypass logic.

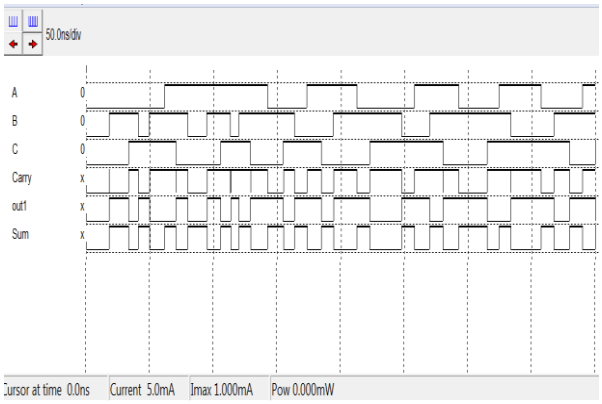

Fig. Timing Simulation for bypass logic base full adder.

This result is known as the Carry-out, which states that an overflow has occurred. The 1-bit FA is an enhanced half adder circuit having an additional Carry in signal, which enables it to be cascaded with other adders and, therefore, is commonly used as a basic building block for generic adder arrays. As the FA is the most widely used structure in a wide range of computationally complex functions, a significant amount of research effort was made on the realization of efficient adder structures.

IV. Parallel Adders

Parallel adders also called as ripple carry adder are digital circuits that perform the addition of two binary strings of equivalent or different size in parallel. The parallel adder is design by series connection of full adders (FA) blocks. Each full adder adds two binary digits at any stage of the ripple carry. The carryout of one stage is fed directly to the carry-in of the next stage. Fig 1 shows an example of a parallel adder: a 4-bit ripple-carry adder. Each bit addition creates a sum and a carry out. The carry out is then transmitted to the carry in of the next higher-order bit. The final result creates a sum of four bits plus a carry out (Sc4).

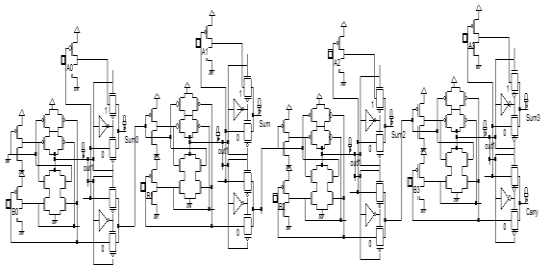

Fig 6 Parallel Adder: 4-bit Ripple-Carry Bypass Logic Adder Block Diagram

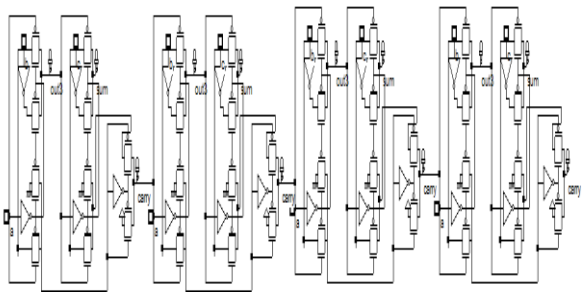

Fig 7 Transmission Gate base Parallel Adder

The major limitation of the parallel adder is that the delay increases linearly with the bit length. As mentioned before, each full adder has to wait for the carry out of the previous stage to output steady-state result.

CMOS Layout Design of Adder With Carry Selection Logic:

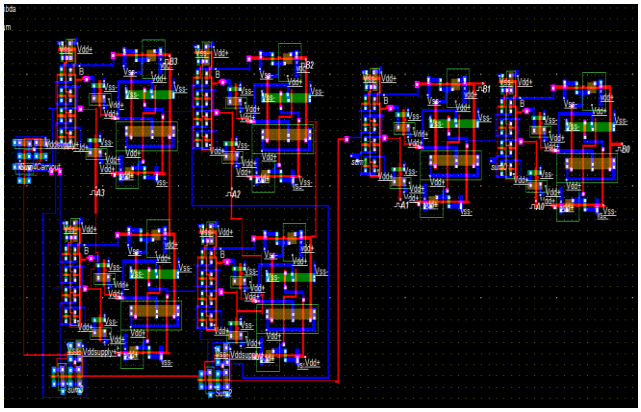

Fig CMOS Layout Design for 4 Bit Adder using Propose Carry Bypass Logic.

The propose CMOS layout of 4 bit adder with carry select logic is shown in fig…….. The three two bit ripple carry adder is design with three 2X1 multiplexer. Channel length of MOSFET is 0.05um and that f channel width is 0.125um. The area of design is 158 um^2. The power dissipation of design is 1.941uW.

Module Design	No. of Transistor	Ouput Load	Power Dissipation	Delay (Tr/Tf)	Area
4 bit CSA with Bypass logic	174	0.38 fF	1.941 uW	.005/0.001ns	158 um^2

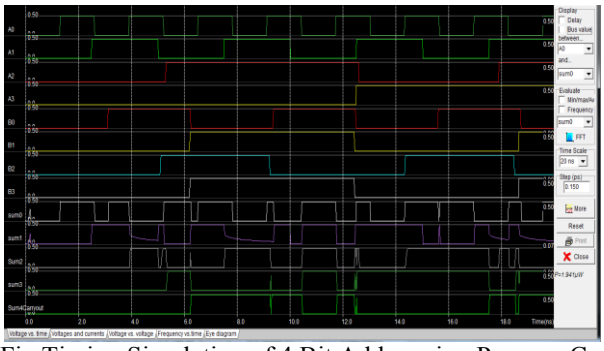

Fig Timing Simulation of 4 Bit Adder using Propose Carry Bypass Logic.

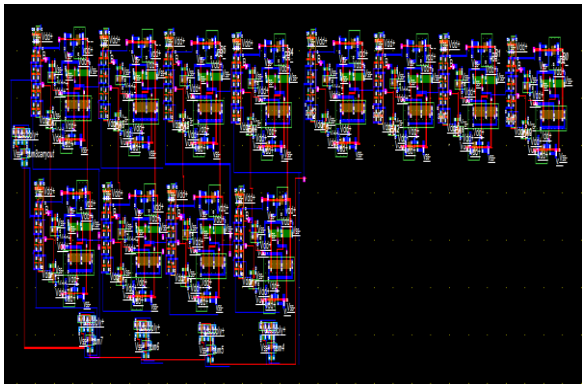

Fig CMOS Layout Design for 8 Bit Adder using Propose Carry Bypass Logic.

The propose CMOS layout of 8 bit adder with carry select logic is shown in fig…….. The three four bit ripple carry adder is design with five 2X1 multiplexer. Channel length of MOSFET is 0.05um and that f channel width is 0.125um. The area of design is 158 um^2. The power dissipation of design is 1.941uW. The design iof 8 Bit Adder using Propose Carry Bypass Logic have 342 transistors comprises of 171 NMOS and 171 PMOS transistor.

Module Design	No. of Transistor	Ouput Load	Power Dissipation	Delay (Tr/Tf)	Area
8 bit CSA with bypass logic	342	0.38fF	3.675 uW	.005/0.001ns	271.875 um^2

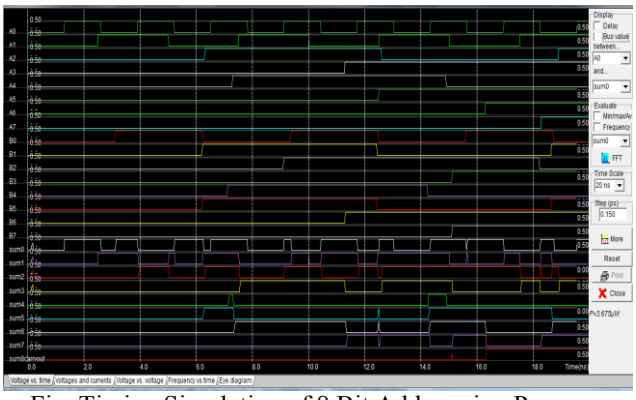

Fig Timing Simulation of 8 Bit Adder using Prapose Carry Bypass Logic.

V. Conclusion

The circuits is simulated in microwind 3.1 using 50nm CMOS technology. A transmission gate base design is an analog switch controlled by logic signals. It uses N and P type MOS transistor. Transmission Gate is a high-quality switch with low resistance and capacitance. Sizing is also not necessary in general, as the resistance and capacitance decrease and increase respectively as the gate W/L ratio is increased. TG is commonly used to implement designs with the minimum number of transistors. In this work the conventional adder using full adder circuits is designed. The propose CMOS layout of 4,8,16,32 and 64 bit adder with carry select logic comprises of group of bit ripple carry adder 2X1 multiplexer. Channel length of MOSFET is 0.05um and that f channel width is 0.125um. The area of design is 158 to 2718 um^2. The power dissipation of design is 1.941uW to 59.374 uW.

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