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Reactive Power Compensation using DSTATCOM with Balanced/Unbalanced Linear and Non-linear Load

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***Abstract* – Presented paper suggests a three phase four wire system observe by balanced/unbalanced linear and non-linear load which similarly connected with the DSTATCOM for which gating signals are furnished with the aid of the influence of pulse generator; it consist a manipulate algorithm for achieving the specified reference current for Voltage Source converter of DSTATCOM using Unit template algorithm technique. The currents injected by the DSTATCOM are controlled in the horizontal vector(d axis) and vertical vector (q axis) using a hysteresis based current control (HBCC) strategy this technique is used to provide the correct getting pulse and collection to the IGBT inverter through comparing error signal with given hysteresis band. By using the HBCC technique the undesired harmonic components are separated from the sensed linear/non-linear load currents. To improvise the output of the controller PI, the comments loop to the integral time period is taken into account In this paper four-leg VSC based DSTATCOM is used for neutral current compensation. The main advantage of four leg VSC is eliminating electrical device at purpose of common coupling (PCC) that conjointly reduce price of DSTATCOM. The results verify the performances taken into considered theoretically for the DSTATCOM topology in MATLAB /Simulink.**

***Keywords* – DSTATCOM, Hysteresis Band Current Controller (HBCC), Proportional Integral Controller (PI), Power Quality (PQ).**

I. INTRODUCTION

In electricity system, frequency fluctuation trouble is a worldwide problem and dealt globally. Power quality is a concern that becomes gradually vital to electricity customers in all respective degree of usage.

The growing range of power electronics based equipment has dangerously impacted the exceptional of electric power supply. With each linear load in system, harmonics are produced which reduces power quality. The indicate the harmonic in strength supply system gives a severe power quality issues that consequences in greater power losses in the distribution system and liable for operation disasters of electronic equipment. As in three phases the 5th, 7th and 11th order harmonics are greater dominating so the current wave is not pure sin wave. To introduce dynamic and adaptable result of such power quality disturbances, efforts are continue by means of the affect of power electronic devices, FACTS, filters and different type of control technique to compensate the power quality problems. The performance of DSTATCOM depends on the selection of interfacing of ac inductor, DC bus capacitor and IGBT. Various researches presenting a complete evaluate on compensating device for improvement of power quality from the system. By using active power filters, synchronous condensers, passive filters, compensating devices such as shunt compensating device (DSTATCOM) series compensating device (DVR) and hybrid of shunt and series compensating device (UPQC) [1, 2]. Proper resolution for all that on top of mentioned issues is solved in planned system victimization Distribution Static Compensation (DSTATCOM) for grabbing this profit [3].

Voltage sag and voltage swell are a number of such problems. Voltage sag is caused by a fault within the utility system, a fault within the purchases facility or a outsized increase of the load current, like starting a motor or transformer energizing. Typical faults are single-phase or multiple-phase short circuits, with the lead to high currents. The high current lead to a drop voltage drop over the network impedance. At the fault location the voltage within the faulted phases drops on the brink of zero, whereas within the non-faulted phases it remains more or less unchanged. To mitigate the power quality problems, many research works are developed within the custom power devices. Transistors (IGBT), a coffee cost microprocessors and techniques developed in the area of power electronics. This problem are often mitigated by installing a custom power device called Distribution Static Compensator (DSTATCOM). This work uses SRF theory for generating reference signals. The DC voltage regulation is a crucial part of STATCOM operation and a easy PI controller is employed for this. The pulses are generated using simple hysteresis control which may be implemented easily. Simulations are performed to verify the performance of the developed system and its results show the efficacy of the system.[4] The proposed system was studied,designed and modeled in MATLAB/Simulink package with a DSTATCOM to simulate its behavior and compensate the harmonics current inject by the loads. The results obtained showed that the proposed SRF control algorithm for four-leg VSC based DSTATCOM has been designed to provide to require desired waveforms as a results for load balancing, reactive power control, neutral current compensation and compensation of current harmonics, under three phase four wire linear balanced and unbalanced linear system [6 7 8].

II. System Description

The system represents a three phase four wire system main components of system are Source followed by a VI measurement, nonlinear load for balance and unbalanced system and there is a DSTATCOM connected in parallel for which gating signals are provided by the pulse generator also including subcomponents as, Voltage source inverter, Capacitor at dc link, Reference current generator and current controller shown in Fig. 1.

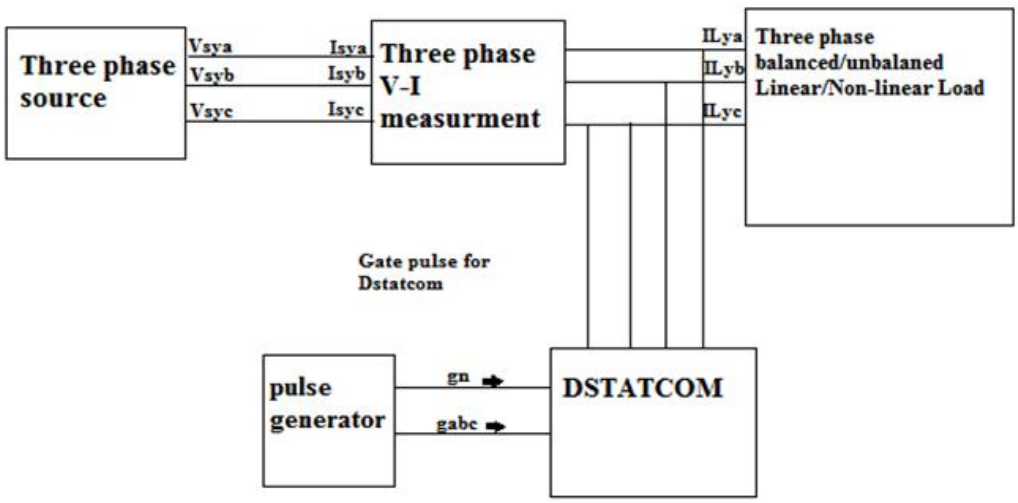

Fig. 1. Block diagram of system.

DSTATCOM consists of a typical three-phase Insulated Gate Bipolar Transistor (IGBT) based four leg VSC bridge with the dc bus capacitor. An extra leg is added to control the current in neutral wire [3]. DSTATCOM is used for instant monitoring of load current, improvement of power factor, regulation of voltage along with, elimination of harmonics, current compensation and maintaining the linear and nonlinear loads also generation

of reference compensating current [4]. The gate pulse of generator used for giving the gate pulses to the VSC of DSTATCOM also as well as for the neutral. In this block all the control pulses exists and also consist Reference current generation, PI controllers, HBCC, PLL etc [5] Algorithm of PI controller involves two separate parameters: The Proportional parameter determines equation of the current error; Integral parameter determines the equation based on the sum of recent errors. Correct regulation of proportional controller's value plays an important role in DC voltage control system's response. Too much increase in proportional gain may results in unsteadiness (fluctuations) on top of system and an excessive amount of much reduction decreases the responding speed system. Further the Integral gain of controller modifies the steady state error. Hence the system becomes stable only at a particular regulated value of PI controller [8, 12]. Many techniques of generation of gating pulses but the most widely used technique is hysteresis controller because of this simplicity and quick response. In hysteresis controller the reference current which was obtained by SRF technique is compared with the filter current and provides the gate pulses for DSTATCOM [11-14].

III. METHODOLOGY

A. *System Configuration and Principle of Operation*

The schematic diagram of four-leg VSC based mostly DSTATCOM feeding three-phase four-wire linear load at the side of unit-template algorithmic is shown in Fig. 2. The distribution system linear loads consist of 3-phase star-connected resistive load and linear loads can produce of three single-phase diode bridge rectifiers with R-C load. These non-linear loads in the distribution system will create PQ issues at the supply while not DSTATCOM. To mitigate PQ issues a DSTATCOM is connected at PCC. The projected DSTATCOM consists of four-leg IGBT based mostly voltage supply converter (VSC), four interface inductors and a dc bus capacitor. The four-leg VSC based mostly DSTATCOM can inject compensating currents (ica, icb, icc) in such some way that supply current (isa, isb, isc) is pure curved and maintains unity PF at supply. A ripple of Resistance (Rf) and Capacitor (Cf) is connected at PCC to filter voltage harmonics at 3-phase source voltages (vsa, vsb, vsc).

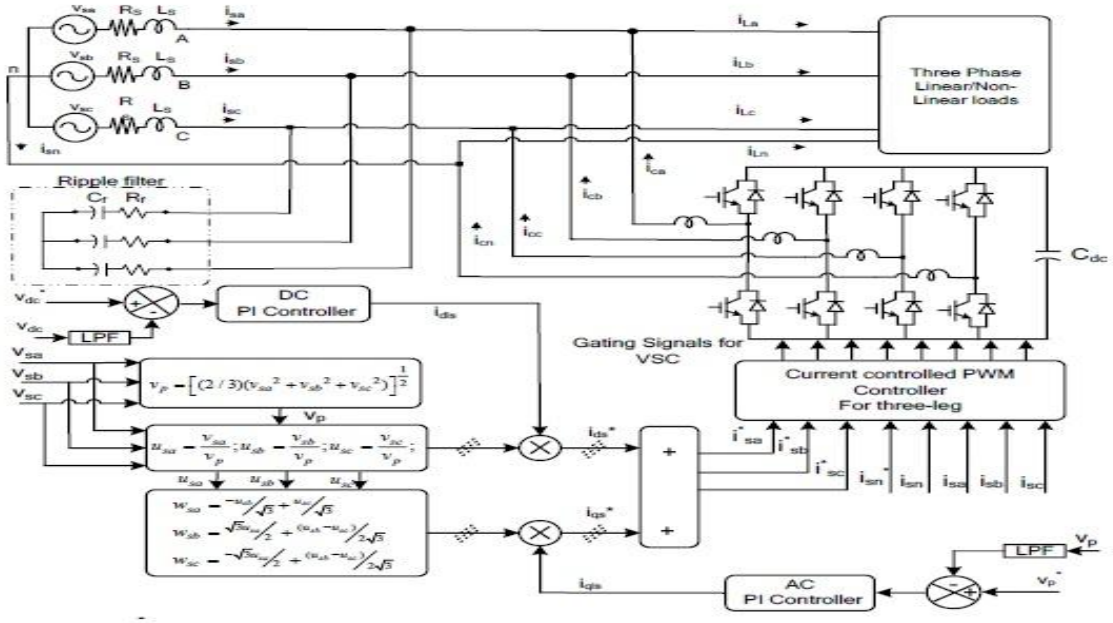

Fig. 2. Diagram of Vsc based Dstatcom with Hysteresis current control technique.

B. *Proposed Hystresis Band Current Control Method*

Fig. 3. appearance hystresis band current control technique. The performance of DSTATCOM depends upon fast and correct extraction of elementary of supply current harmonic elements. All basic control algorithmic of custom power devices needs 10 feedback sensors whereas projected control algorithm needs solely 5 feedback sensors. The fundamental management algorithm need 3 feedback sensors for load currents, 3 feedback sensors for supply voltages, one feedback device for dc bus voltage and 3feedback sensors for supply currents. The unit-template algorithm needs 2 feedback sensors for supply voltages (vsa, vsb), one feedback device for dc bus voltage (vdc) , 2 feedback sensors for supply currents(isa,isb) and conjointly third phase voltage vsc(-(vsa+vsb)) & current isc(-(isa+isb)).The main feature of unit template algorithmic is to reduce range of feedback sensors which may improve performance of DSTATCOM. The planned unit-template control algorithmic primarily based DSTATCOM is that the effective clarification to mitigate harmonics, power factor correction, load unbalancing, reactive power determination and neutral current compensation [11].

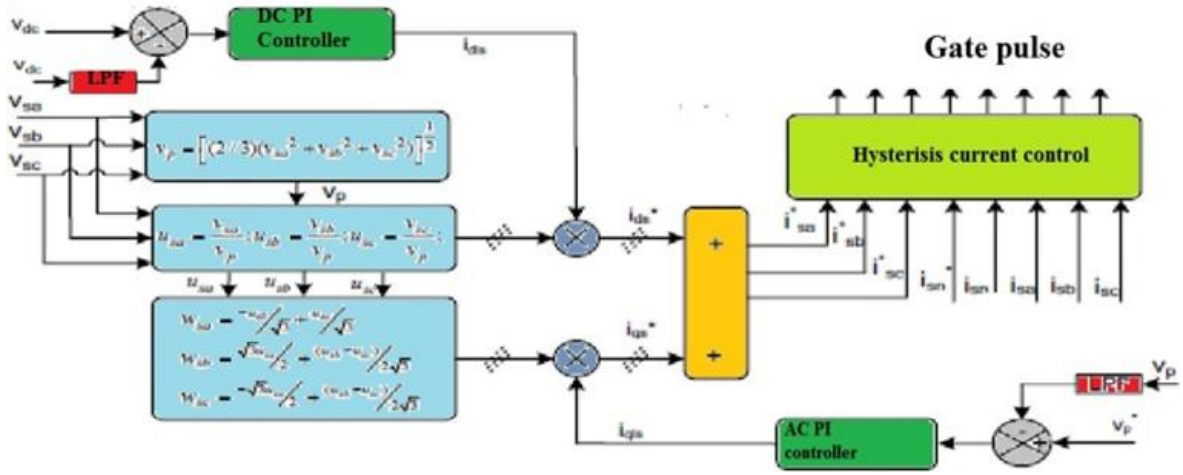

Fig. 3. Hysteresis band current control strategy.

The supply voltages (vsa, vsb, vsc) of three-phase system are typically diagrammatic as,

$$v_{sya} = v_{mp}\ Sin(wt) \tag{1}$$

$$v_{syb} = v_{mp}\ Sin(wt - 120^0) \tag{2}$$

$$v_{syc} = v_{mp}\ Sin(wt - 120^0) \tag{3}$$

The magnitude of 3 phase voltages (vsa, vsb, vsc) at PCC is given by

$$v_t = \sqrt{\frac{2(v_{sya}^2 + v_{syb}^2 + v_{syc}^2)}{3}} \tag{4}$$

Correction Operation of Unit Template based DSTATCOM

The in-phase part of unit templates (usa, usb, usc) are calculated from (vsa, vsb, vsc) that are given by,

$$u_{sa} = \frac{v_{sya}}{v_t}; u_{ba} = \frac{v_{syb}}{v_t}; u_{ca} = \frac{v_{syc}}{v_t} \tag{5}$$

The dc bus voltage error (vedc) is that the distinction between reference dc bus voltage (vdc*) and precived dc bus voltage (vdc) underneath PFC mode. This dc voltage error is given to dc bus Proportional Integral (PI) c-

-ontroller and its output of PI is taken under consideration as active factor of current loss (idls).

$$i_{dis\,(k)} = i_{dis\,(k-1)} + K_{dp}\left(v_{edc\,(k)} - v_{edc\,(k-1)}\right) + K_{di}\,v_{edc\,(k)} \quad (6)$$

Where Kdp and Kdi are proportional and integral gain constants of DC bus PI controller. The reference active part supply currents (idsa*, idsb*, idsc*) are determined as,

$$i^*_{dsa} = u_{sa}\,i_{dls}\,; i^*_{dsb} = u_{sa}\,i_{dls}\,; i^*_{dsc} = u_{sc}\,i_{dls} \quad (7)$$

The quadrature phase section part of unit templates (w_{ya},w_{sb},w_{sc}) are calculated from (u_{sa}, u_{sb}, u_{sc}) that are given by,

$$W_{sya} = \frac{(-u_{sb} + u_{sc})}{\sqrt{3}}; \quad (8)$$

$$W_{sb} = \frac{(-\sqrt{3}u_{sb} + u_{sc} - u_{sc})}{2\sqrt{3}}; \quad (9)$$

$$W_{sc} = \frac{(-3u_{sa} + u_{sb} - u_{sc})}{2\sqrt{3}} \quad (10)$$

The ac bus voltage error (vep) is the distinction between reference ac bus voltage (vt*) and perceived ac bus voltage at PCC. This ac voltage error is given to ac bus Proportional Integral (PI) controller and its output of PI is taken under consideration thought-about as reactive part of current loss (iqls).

$$i_{qis\,(k)} = i_{qis\,(k-1)} + K_{qp}\left(v_{ep\,(k)} - v_{ep\,(k-1)}\right) + K_{qi}\,v_{ep\,(k)} \quad (11)$$

Where Kqp and Kqi are proportional and integral gain constants of AC bus PI controller. The reference reactive part supply currents (iqsa*, iqsb*, iqsc*) are determined as,

$$i^*_{qsa} = w_{sa}\,i_{qls}\,; i^*_{qsb} = w_{sb}\,i_{dls}\,; i^*_{qsc} = w_{sc}\,i_{qls} \quad (12)$$

C. *Generation of Reference Supply Currents*

The total reference source currents (isa*, isb*, isc*) are the sum of the reference in-phase source current (idsa*, idsb*, idsc*) and reference quadrature source currents (iqsa*, iqsb*, iqsc*) are

$$i^*_{sa} = i^*_{dsa} + i^*_{qsa} \quad (13)$$

$$i^*_{sb} = i^*_{dsb} + i^*_{qsb} \quad (14)$$

$$i^*_{sc} = i^*_{dsc} + i^*_{qsc} \quad (15)$$

D. *Current Controlled PWM Generator*

In a current controlled PWM Generator, the distinction between reference supply currents (isya*, isyb*, isyc*) and perceived supply currents (isya, isyb, isyc) are taken as error supply currents in every of the three phases. In additionally to error supply currents in 3 phases, the supply neutral currents (isn) are compared with triangular waveform to get change pulses for four-leg VSC based mostly DSTATCOM [12].

E. *Design of DSTATCOM*

The planning of an system becomes a challenging task for meeting the strict requirements of critical loads. The utilization of MATLAB software for the planning stage helps in providing enhanced understanding of the

circuit behavior, selection of component parameters and ratings; designing of closed loop system sort of controllers, and also to realize the simplest best outcomes and exact solutions for the system. The dimensions of the capacitance connected doesn't play a that much vital role in generation of reactive power, it provides costs at a substaintial amount also reducing the general size of the compensator and overall cost of the system. These loads probably be a lagging power factor sort of load. For reducing ripple contents from the system compensated currents, appropriate value of inductance (Lf) are used at AC side of the DSTATCOM. A resistor (f) connected in parallel and capacitor (Cf) connected in series represents ripple filter which must be connected common coupling point (PCC) with the loads and therefore the compensator to filter at the high frequency switching distortions in voltage profile at PCC. The harmonics components of currents (Icc) are injected by the DSTATCOM to eliminate the harmonic components of the load current hence the source currents are free from distortion and compensation of reactive power is completed [3]. The particular rating of the ripple filter, AC inductors, DC bus voltage, DC bus capacitor of DSTATCOM are calculated as, calculation for dc link voltage.

The rating of DC link bus voltage ($Vdcl$) depends upon the common coupling point (PCC) voltage and it must be high than the peak of the line voltage for desired optimization of the pulse width modulation of VSC of DSTATCOM, therefore the Voltage at dc link $Vdcl$ is calculated as, $Vdcl = 2 \times \sqrt{2}\ (Vdcl / \sqrt{3} \times Ma) = 677.7V$ (17) where Ma is modulating index which is equal to 1. The voltage of the DC link is preferred as 700V. $Vdcl$ is that the AC line output voltage of DSTATCOM putting as 677.7 V.

Design of DC Link Capacitor:

$Vdcl$ is the standard dc voltage value, I is that the current at phase of the DSTATCOM, Vpya is that the voltage at phase and t is time that DC bus voltage is to be settled value of k factor is varying between 0.05 to 0.15. The worth of Capacitor at dc link is calculated as $Cdc = 0.5Cdc\ \{(Vdcl\ 2) - (Vdcl1\ 2)\} = k\{3\ Vpx\ (aI)\ t\}$ (18) Put values of a = 1.2, Vpxa = 240V, $Vdcl$ = 677.69V, Vdc = 700V, at time t = 0.04s, and also the approximate value of Cdc is found to be 6622.22 µF and it's selected as 10000 µF.

Ripple Filter

A first order low pass filter shown in tuned at the switching frequency which may be used further to filter out the low frequency losses from the voltage at the PCC. A inductor connected in series with resistance is chosen as a ripple filter. The worth of capacitor of the ripple filter and resistance are measured as 4mH and 0.1 Ω respectively [3, 4, 5].

IV. Results and Discussion

A. *Balanced Non-linear Load*

The analysis of hysteresis band current control technique based DSTATCOM under balanced non- linear load conditions, and various results are calculated after simulation briefly in below.

Under balanced system timings of circuit breakers just like one other also the load must having identical load parameters. At time t = 0s to time t = 0.3s the controller is off so therefore waveform of uncompensated source current flow but After 0.3 s, the DSTATCOM was switched on and therefore the output waveform setting down at time t = 0.3 sec, the THD was 31.42% which is intolerable hence the harmonic distortion analysis of supply current after compensation THD measured as 4.69%.

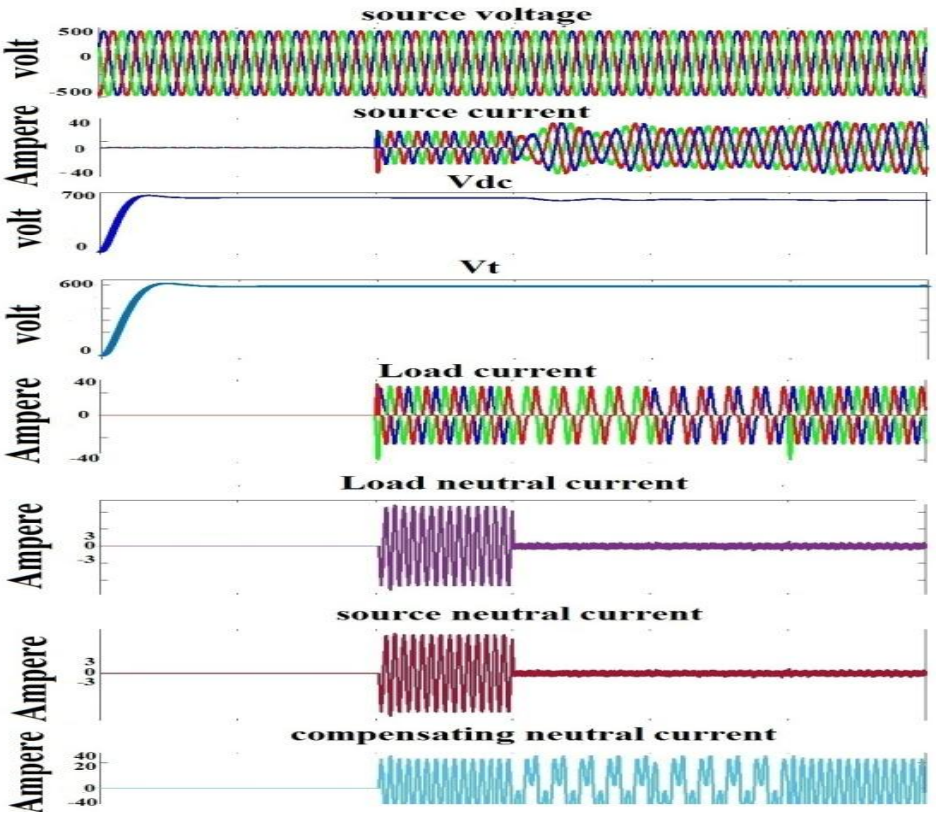

Fig. 4. Output waveforms for balanced Non-linear load.

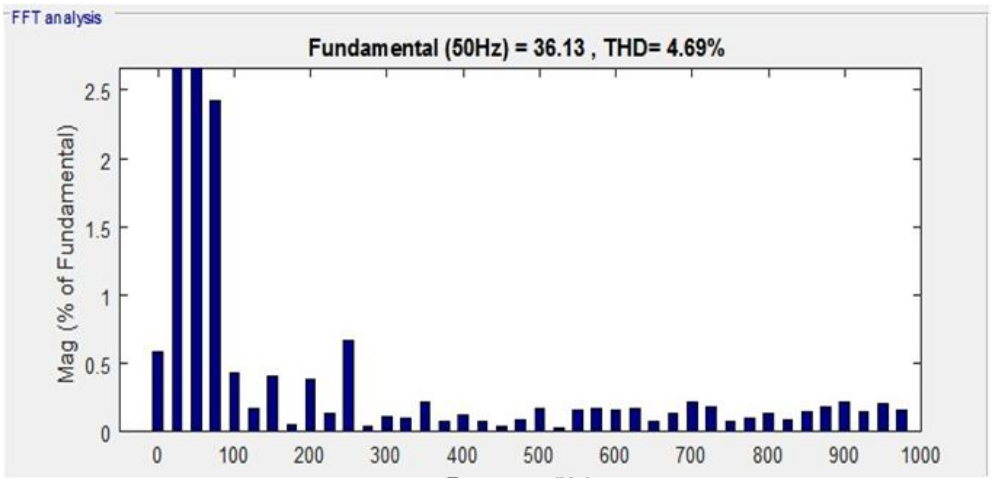

Fig. 5. Frequency analysis of source current waveform for balanced load shown 4.69% THD.

B. *Unbalanced Non-linear Load*

Firstly in unbalanced load conditions the load parameters must be varied from each other also the switching timings of circuit breaker are different from each other and must be followed a simultaneous triggering pattern, after complete analysis we found that the supply currents are balanced, in-phase with the supply voltage at phase, sinusoidal wave and free from distortion also the harmonic current is compensated. When the DSTATCOM is switched on at time t = 0.3s, the voltage waveforms and compensating current is found to be in phase. Fig. 7 shows the Fourier transform analysis for unbalanced nonlinear load, the THD was 31.42% which is intolerable hence the harmonic analysis analysis of supply current after compensation should be measured as 4.69%.

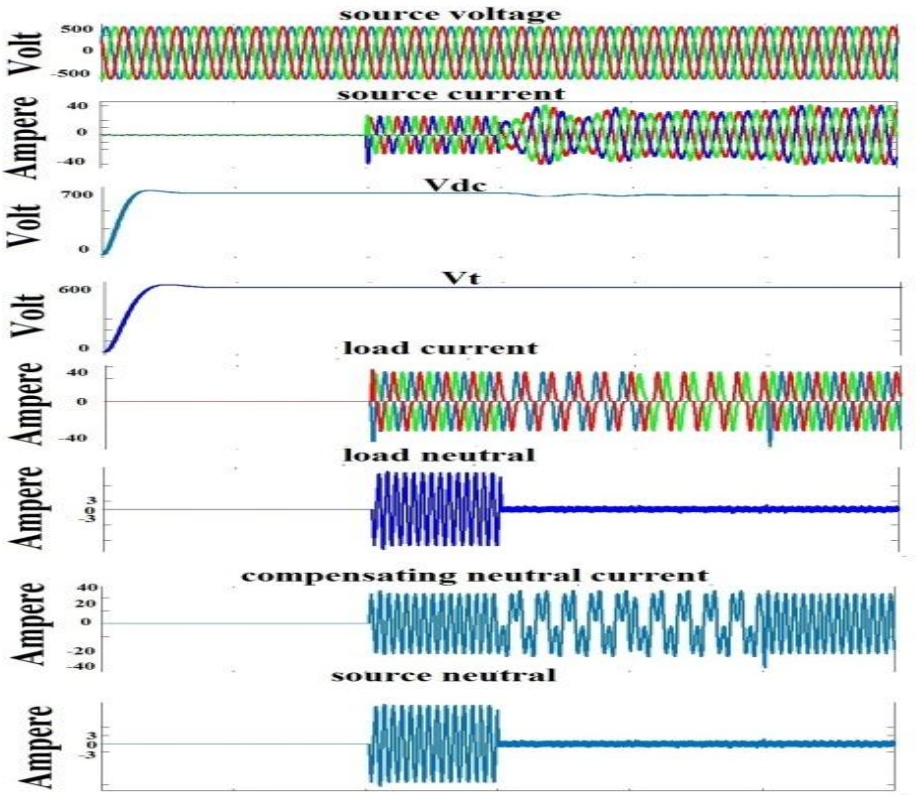

Fig. 6. Output waveforms for unbalanced Non-linear load.

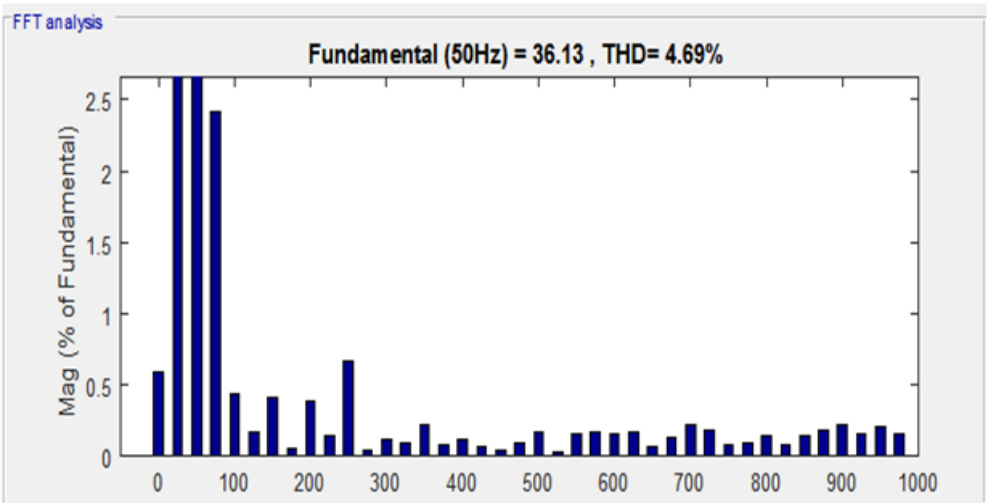

Fig. 7. Frequency analysis of compensated source current for unbalanced load shown 4.69% THD.

C. *Balanced Linear Load*

The analysis of hysteresis band current control technique based DSTATCOM under balanced linear load conditions, and various results are calculated after simulation briefly in below.

Under balanced system timings of circuit breakers just like one other also the load must having identical load parameters. At time t = 0s to time t = 0.3s the controller is off so therefore waveform of uncompensated source current flow but after 0.3 s, the DSTATCOM was switched on and therefore the output waveform setting down at time t = 0.3 sec, the THD was 39.16% which is intolerable hence the harmonic distortion analysis of supply current after compensation THD measured as 4.71%.

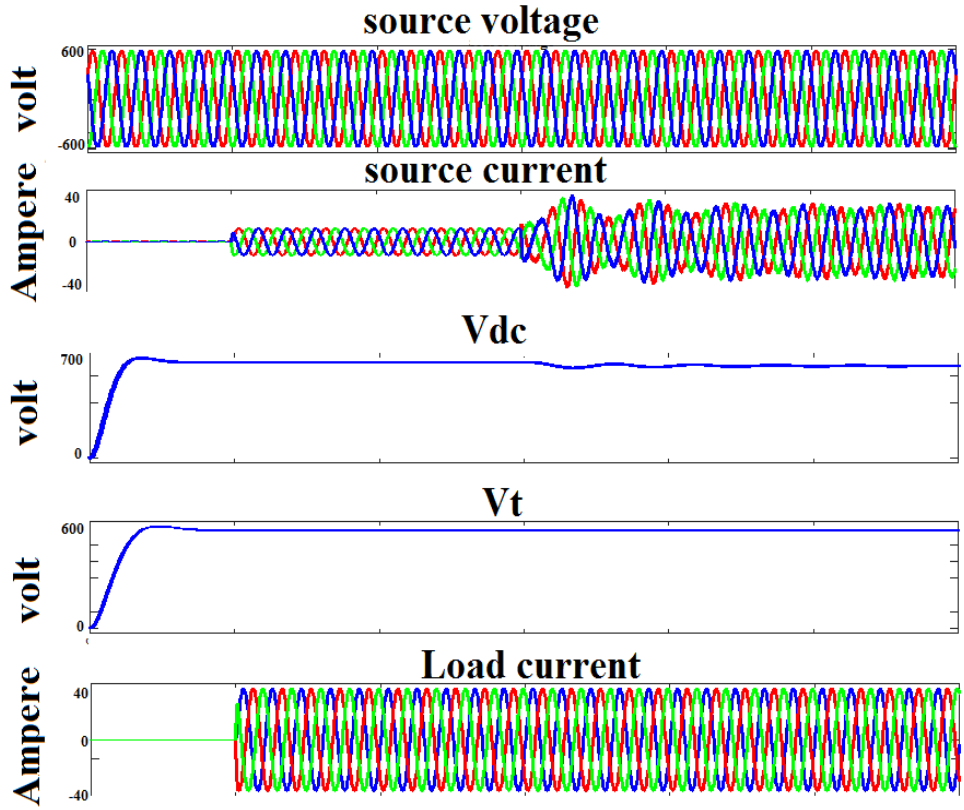

Fig. 8. Output waveforms for balanced linear load.

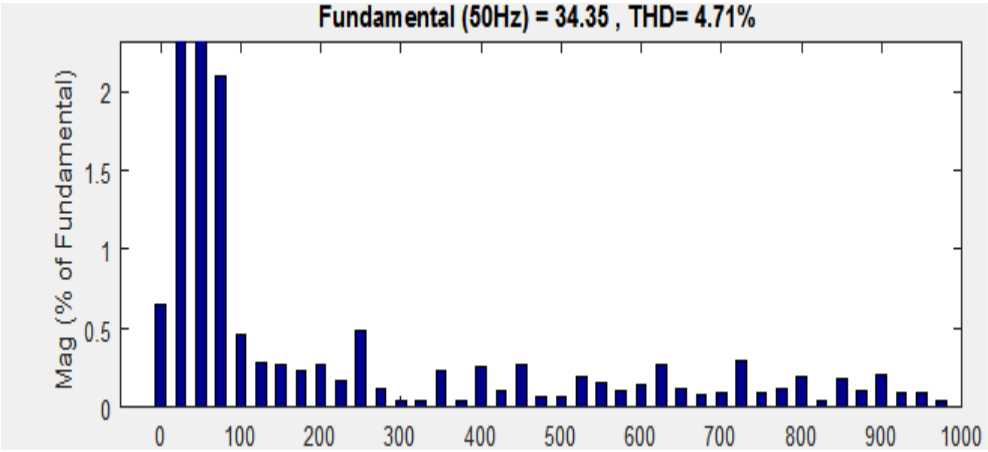

Fig. 9. Frequency analysis of source current waveform for balanced load shown 4.71% THD.

D. *Unbalanced Linear Load*

Firstly in unbalanced load conditions the load parameters must be varied from each other also the switching timings of circuit breaker are different from each other and must be followed a simultaneous triggering pattern, after complete analysis we found that the supply currents are balanced, in-phase with the supply voltage at phase, sinusoidal wave and free from distortion also the harmonic current is compensated. When the DSTATCOM is switched on at time t = 0.1s, the voltage waveforms and compensating current is found to be in phase. Fig. 11 shows the Fourier transform analysis for unbalanced linear load, the THD was 31.42% which is intolerable hence the harmonic analysis analysis of supply current after compensation should be measured as 5.73%.

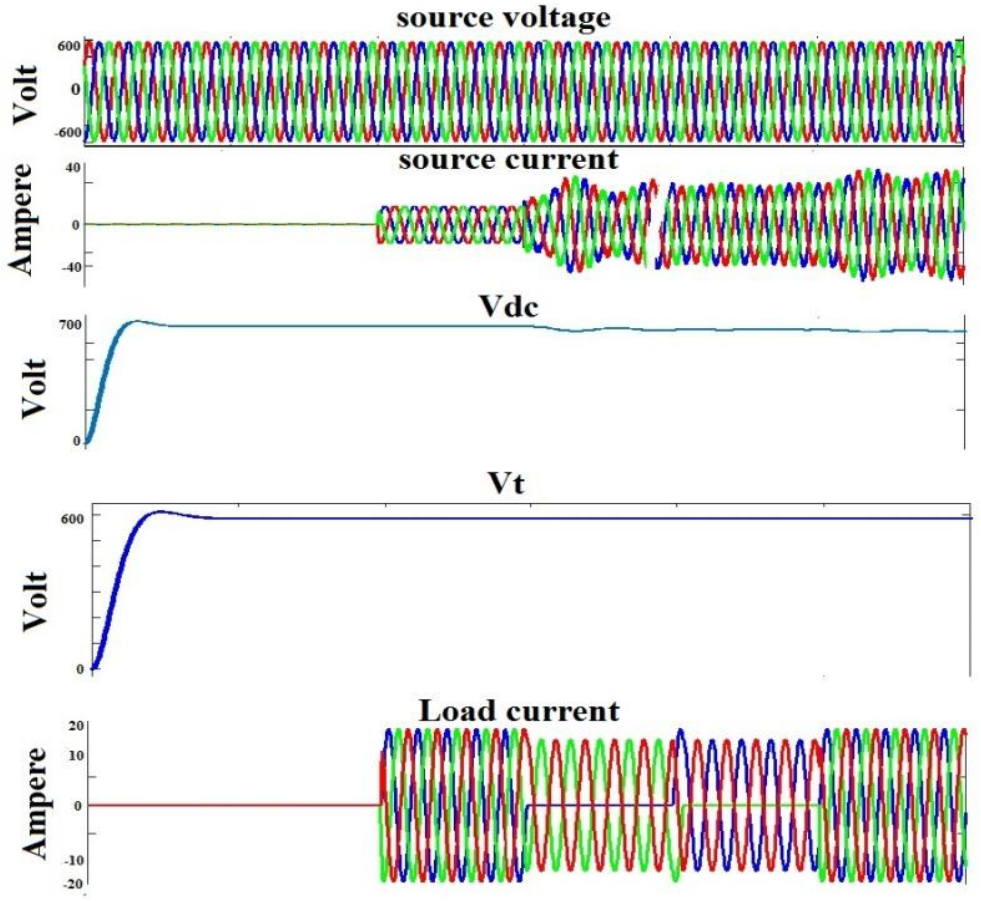

Fig. 10. Output waveforms for unbalanced linear load.

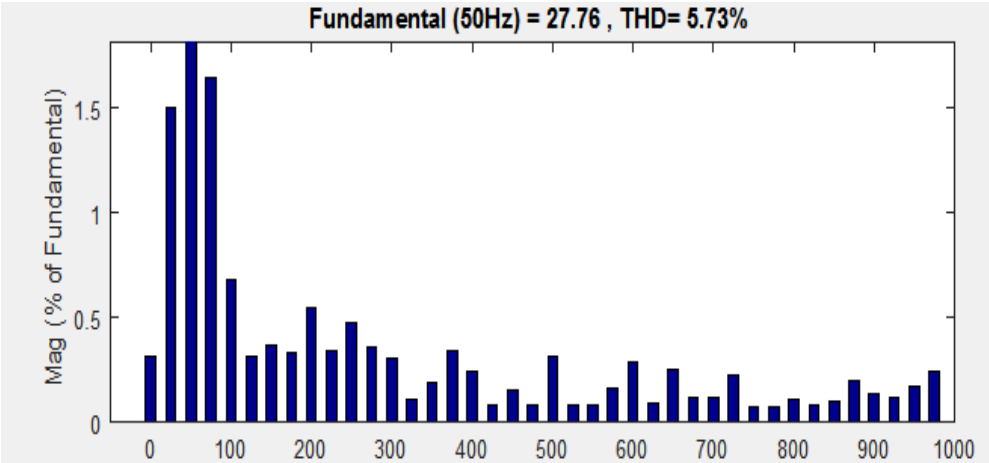

Fig. 11. Frequency analysis of compensated source current for unbalanced load shown 5.73% THD.

V. CONCLUSION

Hysterisis band current control technique which can be used for the generation of gating pulses for four-leg DSTATCOM for three-phase four-wire distribution system to improve the distortion and harmonic components created in the system under variable distorted linear balanced and unbalanced and non-linear balance and unbalanced load conditions. The model was developed using Simulink and Sim Power System toolbox. The simulation is performed for balanced as well as unbalanced linear and non-linear loads. It was seen that before the compensation was provided, the current and therefore the voltage waveforms were out of phase. Further the

HBCC based DSTATCOM is connected in the network, the current compensation was provided, making the current and voltage waveforms in phase and must be sinusoidal. The following objectives have been successfully achieved.

- Load balancing.
- Harmonics Current Compensation.
- Voltage Regulation.

Fig. 7. Output waveforms for unbalanced linear load.

APPENDIX

Table I. Simulation output performance parameters.

Parameters	Unit	Balanced Linear Load	Unbalanced Linear Load	Balanced Non-linear Load	Unbalanced Non-linear Load
Vs	Voltage	586.7v	586.7v	586.6V	586.8V
Is	ampere	31.91A	25.64A	36.13A	36.13A
Vdc	Voltage	700v	700v	700v	700v
Vt	voltage	600v	600v	600v	600v
In	ampere	0	0	2.2A	2.5A
THD	%	4.71%	5.73%	4.69%	4.69%

Three phase supply voltage = 415V, 50Hz.

Supply Impedance: Rs = 0.01Ω, Ls = 1mH.

Unbalanced/ Balanced Linear and non-linear loads: Three single phase diode bridge rectifier R = 25Ω and L = 8mH C = 100 μF.

DC bus Capacitor Cdc = 4500 μF DC bus PI Controller: Kp = 0.9, Ki = 0.08

AC bus PI controller: Kp = 0.5, Ki = 0.9

Low pass filter: 20Khz pf: 0.707

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