

# Modeling of the Transfer Characteristics for High Series Resistance in Nanoscale FD SOI MOSFET Devices

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**Abstract** – This study presents a unified electrical model for a Nanoscale FDSOIMOSFET with a channel thickness as low as 1.6 nm. The experimental I-V Transfer Characteristics are anomalous in the linear region. This phenomenon is modeled by a huge parasitic drain-source series resistance, dependent on the gate voltage. Moreover the gate leakage current is included in this generic model. Additional methods, like CV and Rm-L, were used to indicate the origin of the series resistance. The generic analytical approach developed in this model can be useful for the Nano-Scale Body (NSB) devices modeling, where such phenomena are of great reliability concern to guide Failure Analysis (FA) of FDSOI MOSFET and Transistor-like Nanoscale Devices Regime.

**Keywords** – Analytical Model, I-V & C-V Characteristics, Nano-Scale Body (NSB) and Ultra-Thin Body (UTB) FDSOI MOSFETs Devices, Series Resistance and Mobility.

## I. INTRODUCTION

Nanoscale Silicon-On-Insulator (SOI) Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) based devices are the building blocks of up-to-date systems allowing ultra-fast data processing. This is in accordance with efforts to develop new generations of ultra-fast computers based on combined electronic and signal processing on one hand[1], and advanced generations of Nano-Scale Body devices (NSB) for communication systems [2,3] on the other hand. In this article, we propose an accurate analytical model to explain the anomalous behavior of NSB SOI MOSFETs with channel having a thickness as low as 1.6nm and recess channel structure [4].

## II. DEVICE PROCESSING AND CAD SIMULATION

### A. Desirable SIMOX Wafer Processing Technology

Several techniques were developed in the past to create Silicon-On-Insulator (SOI) devices [5-7], since their implementation was found promising [8] for ULSI [9], low power [10], military and space [11], and cost reducing [12] applications. In this research, commercial (SOITEC) 6" diameter Separation-by-IMplanted-OXYgen (SIMOX) SOI wafers were chosen as the starting material. This is universally known that more advanced SOI technologies were developed the past for the industry, like the UNIBOND™ line of SOI wafers created using the Smart Cut® process technology, allowing thickness uniformity. However, for research purpose, this SIMOX technology has the clear advantage of presenting an initial gradient of

the silicon thickness across the same wafer. This desirable gradient can be conserved during the NSB fabrication process, making it possible to study the thickness variation influence on electrical characteristics.

### B. Mapping of the Silicon Gradient

Using a visible light spectrophotometer (FT750) which allows multilayer thin films measurements (with layers typical thickness ranging down to 10 nm), we mapped the thickness of the SOI initial layer over the 6" SIMOX wafer, and found it varying between 49.83 to 59.40 nm (Fig.1.a). Usage of complementary thin films measurement methods like ellipsometry, and HRTEM was found to reinforce the thickness results with very high precision. To face our process tooling constraints, 2" diameter wafers had to be cut from the initial 6" SIMOX wafer. The largest thickness gradient zone (located at the opposite edge of the wafer flat) has been selected to be cut. After completing the thinning process (described below) the thickness of the silicon channel was mapped and was found varying between 1.64 to 6.57 nm (Fig.1b). The surface uniformity of 1.6nm was definitely measured near the wafer's flat on two adjacent dies covering both an area of about 10 mm<sup>2</sup>.

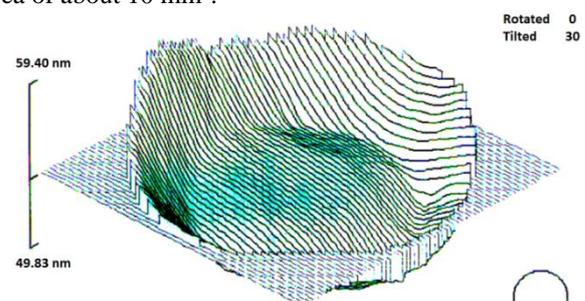


Fig.1.a. Map of the initial 6" diameter SIMOX wafer, showing the variation of the original SOI thickness from 59.40 nm to 49.83 nm.

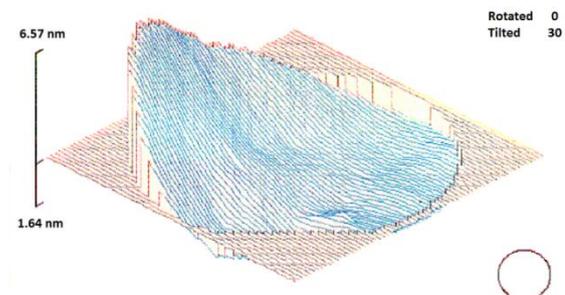


Fig.1.b. Map of the 2" diameter wafer cut from the edge of the previous wafer showing the variation of the thinned silicon channel from 6.57 nm to 1.64 nm.

### C. Control of the Channel Thickness Uniformity

The most challenging step was the accurate and controlled thinning process of the SOI layer using local oxidation until reaching a 1.6 – 6.5nm range of thickness, while the source and the drain regions remained in their original thickness. In order to check the capability of accurate thinning, preliminary tests of thinning were performed in order to reach thicknesses lower than 10nm, when characterizing the furnace parameters like furnace temperature, duration of the oxidation, and growth rate [13].

The study focused on the thinnest available device (1.6 nm) in which we hypothesized that the parasitic phenomena would be better expressed. The thickness value was confirmed by the HRTEM cross section and found uniform all along the device (see Fig.2).

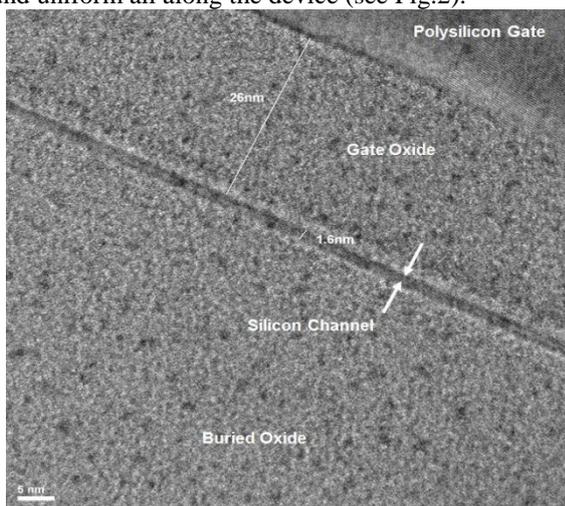


Fig.2. Image of the Si Channel cross-section using High Resolution Transmission Electron Microscope (HRTEM).

### D. TCAD Simulation of the Device Processing

In order to perform a deeper and accurate analysis of the process limitations, the layers deposition process was translated to a model of the device using Crosslight software. One of the main outputs of the simulation are the 2-D and 3D device cross-sections, and which includes among others the exact boundaries of the various layers of materials in the structure. The value of Cross-Light is to highlight the device layers' morphology, and the gate-recessed channel technology, used in the device process.

In figure 3 below, we present a cross-section of the NSB including the Source, Gate and Drain (respectively S, G, and D) parts, and a zoom of the gate-recessed silicon channel. As presented in the upper insert, the active region which is built of layers described above, is terminated by Aluminum contacts (layer 10) in the vertical axis, and limited by Field Oxide (layer 07) borders in the horizontal axis. The Buried Oxide (layer 02) is serving as a barrier between the bulk silicon (layer 01) and the Gate-recessed silicon channel (layer 03).

The lower insert of figure 3 represents a zoom-in of the gate-recessed channel, when the silicon layer was thinned from 46 nm to 1.6 nm minimal thickness, as confirmed by HRTEM picture in figure 2. This points out advantage of

the recessed process in which only the silicon channel is thinned while the source and drain extensions are remaining in their original thickness. The zoom in provides a view of the gate overlap on the thinned channel and over the extensions of the drain and sources regions and their bottleneck with the channel respectively.

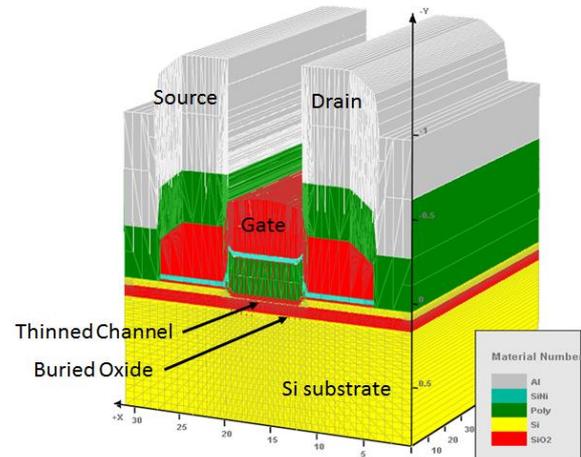


Fig.3.3. D cross view of a Crosslight simulated NSB device using the gate recessed channel process, and showing the five main layers, as well as the thinned channel.

## III. RESULTS

### A. Transfer Characteristics Analysis

Analysis of the Transfer Characteristics yields that Drain ( $I_{DS}$ ) and Gate ( $I_{GS}$ ) currents are simultaneously measured as a function of  $V_{GS}$ , in the range of -2V to 2V for several values of the  $V_{DS}$  Voltage. The  $V_{DS}$  values are selected in the linear domain of operation (0.1V to 0.4V by steps of 0.1V) and short ( $V_{DS} = 0V$ ). Experimental results are shown in fig. 4 (semi-log).

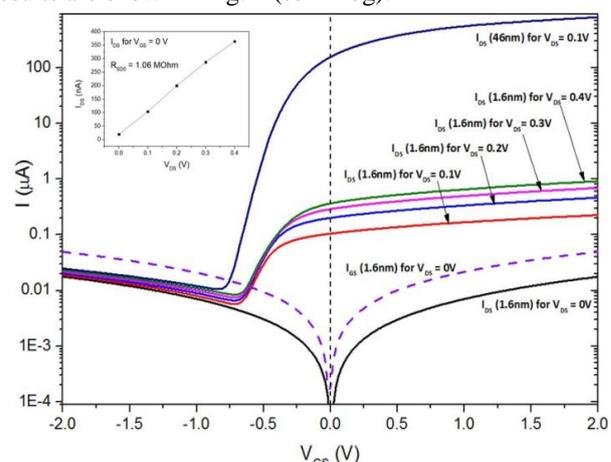


Fig.4. Measured log  $I_{DS}$ - $V_{GS}$  characteristics in the short ( $V_{DS} = 0V$ ) and linear operation mode ( $V_{DS} = 0.1, 0.2, 0.3, 0.4V$ ) for the 1.6 nm thick NSB. The characteristic of the Ultra-Thin Body device (UTB) (non-thinned 46 nm channel thick) is superposed for reference at  $V_{DS} = 0.1V$ . The  $I_{DS}$ - $V_{DS}$  plot for  $V_{GS} = 0V$  is shown in the upper left part for the 1.6 nm thick NSB.

By increasing  $V_{GS}$  from  $-2V$  to  $-0.7V$ ,  $I_{DS}$  slowly decreases, and slightly depends on  $V_{DS}$ , indicating a leakage phenomenon (negative resistance) similar to the Gate Induced Drain Leakage (GIDL) observed for both classic and SOI-MOSFET devices [14]. The “short” measurement ( $V_{DS} = 0V$ ) shows that  $I_{DS}$  is approximately equal to the half of  $-I_{GS}$  for negative but also for positive  $V_{GS}$  values. The leakage current  $I_{GS}$  is found identical for the both devices indicating that the leakage is independent of the channel. This result can be interpreted by the presence of a couple of leakage resistances between the gate-drain and gate-source extremities. These resistances, which are almost symmetrical in the linear region, act as current dividers of the gate current. The value of the gate leakage resistance  $R_G$  is estimated from the average slope of the gate current  $I_{GS}$  vs.  $V_{GS}$  as  $50M\Omega$ .

Above  $V_{GS}$  value of  $-0.7V$   $I_{DS}$  is growing steeply (exponential like), but is strongly bended above  $-0.3V$  and turns into another linear dependence on  $V_{GS}$ . The exponential behavior indicates that the device is operating in a subthreshold mode between  $-0.7V$  and  $-0.5V$ . For the non-thinned (46 nm thick) device, where the measured drain current (at  $V_{DS} = 0.1V$ ), is three orders of magnitude higher the threshold value  $V_T$  is estimated to be  $-0.4V$ .

Since the subthreshold domain of the thinned device is positively shifted by  $0.2V$  relatively to the non-thinned device, the threshold voltage is estimated to be  $-0.2V$ . This result is consistent with the increasing of  $V_T$  by thinning the channel below 10 nm due to quantum mechanics considerations [15].

The zero  $V_{GS}$  values of  $I_{DS}$  characteristics exhibit a linear dependence on  $V_{DS}$  with a reciprocal slope equivalent  $R_0$  of  $1.06 M\Omega$  (see inserted plot in fig. 4). For comparison the equivalent  $R_0$  for the Ultra-Thin Body device (UTB) (non-thinned 46 nm channel thick) is about  $10 k\Omega$  only. In the following we propose a quantitative interpretation for such a huge difference of  $R_0$  resistance.

Assuming no series' resistance,  $R_0$  should be the transistor's intrinsic channel resistance  $R_{ch}$  which is given by the following equation:

$$R_0 = R_{ch} = \frac{L}{W\mu_{eff}C_{ox}(V_{GS} - V_T)} \quad (1)$$

In both devices, the ratio  $W/L$  is  $80/8$  and the front gate oxide equivalent thickness is  $26 nm$ , so the gate capacitance value  $C_{ox}$  is  $138 nF/cm^2$ .

As recently reported in the literature by both measurements [16] and simulations [17] the effective mobility of the electrons ( $\mu_{eff}$ ) is decreasing with the channel thickness: from about  $600 cm^2/Vs$  for  $50 nm$  thick SOI devices to a value of about  $30 cm^2/Vs$  for a  $1.6 nm$  thick SOI-MOSFET [16]. By taking these mobility values into equation (1), the corresponding channel resistances could be estimated to  $3 k\Omega$  and  $120k\Omega$  respectively. The former value is matching the measured  $R_0$  one ( $10 k\Omega$ ) while the latter value is about one order of magnitude lower than our measured value  $R_0$  ( $1.06 M\Omega$ ). Consequently, for the  $1.6 nm$  thick device the difference can be interpreted by an additional series resistance

appearing during the channel thinning process. In a third section of this paper, we will present more experimental methods that will confirm this interpretation. By now, we focus on the development of the analytical model of the transfer characteristics of the NSB.

### B. Transfer Characteristics Modeling

When considering the influence of a series resistance ( $R_{SD}$ ), the drain current in the linear domain is classically expressed by [18]:

$$\text{For } V_{GS} \geq V_T, I_{DS,lin} = \left( \frac{g_{ch}}{1 + g_{ch}R_{SD}} \right) V_{DS} \quad (2)$$

Where  $g_{ch}$  is the intrinsic channel conductance defined par  $1/R_{ch}$  ( $R_{ch}$  expression is given by equation (1)). By considering the following limiting cases of equation (2):

$$\text{For } V_{GS} \geq V_T, \lim_{R_{SD} \rightarrow \infty} I_{DS,lin} = \frac{V_{DS}}{R_{SD}} \quad (3)$$

$$\text{For } V_{GS} \geq V_T, \lim_{R_{SD} \rightarrow 0} I_{DS,lin} = g_d V_{DS} \quad (4)$$

For  $1.6 nm$  thick device, at zero  $V_{GS}$  (larger than  $V_T$  estimated to  $-0.2V$ ), we have shown that the calculated  $R_{ch}$  ( $120 k\Omega$ ) is much lower than  $R_0$  ( $1.06 M\Omega$ ). Then, the difference that we interpret as a series resistance  $R_{SD}$  ( $940 k\Omega$ ) is much higher than  $R_{ch}$ . Consequently the measured  $I_{DS}$  current can be simply expressed by the equation (3).

For high positive  $V_{GS}$  values the linear rise of  $I_{DS}$  observed in figure 5 can be described by a decreasing of  $R_{SD}$  with  $V_{GS}$  as observed in MOSFET's [19] according the following expression ( $V_T$  is here negligible relatively to  $V_{GS}$ ):

$$R_{SD} = \frac{R_{SD0}}{1 + \theta V_{GS}} \quad (5)$$

Then, the linear  $I_{DS}$  function for both  $V_{DS}$  and  $V_{GS}$  variables can be written as:

$$I_{DS,lin} = \frac{V_{DS}}{R_{SD}} = \left( \frac{1 + \theta V_{GS}}{R_{SD0}} \right) V_{DS} \quad (6)$$

The corresponding transconductance  $g_m$  is derived from the above equation as:

$$g_m = \left. \frac{dI_{DS}}{dV_{GS}} \right|_{V_{DS}} = \frac{\theta}{R_{SD0}} V_{DS} \quad (7)$$

By plotting the measured  $g_m$  vs.  $V_{DS}$  the value of  $\theta$  can be estimated to  $0.70$  while  $R_{SD0}$  is taken to  $1.06 M\Omega$  as mentioned above. Finally it is derived that all over the measured  $V_{GS}$  range,  $I_{DS}$  is a combination of three currents. The first one is  $I_{DS,lin}$  as mentioned in (3), and is still dominant above  $V_T$  since the intrinsic channel resistance is still negligible when compared to  $R_{SD}$ . The second current is due to a subthreshold ( $V_{GS} < V_T$ ) (diffusion) current expressed as following:

$$I_{DS,sub} = I_{DS0} e^{\frac{q}{nkT}(V_{GS} - V_T)} \quad (8)$$

An exponential fit of the measured  $I_{DS}$  vs.  $V_{GS}$  between  $-0.5V$  and  $-0.3V$  is used to extract the parameter  $n$  (ideality factor) which is found as  $3.6$  and  $3.8$  for  $V_{DS}$  values of  $0.1$

V and 0.4 V respectively. The extracted pre-factor current  $I_{DS0}$  equals to 709 nA and 894 nA respectively, and is expected to be 0 at zero  $V_{DS}$ . The third current is the half of the gate leakage  $-I_{GS}$ , and acts as a baseline.

The total current can be then modeled in the whole  $V_{GS}$  measurement domain by the following general expression:

$$I_{DS,total} = \frac{I_{DS,lin} \cdot I_{DS,sub}}{I_{DS,lin} + I_{DS,sub}} - \frac{V_{GS}}{2R_G} \quad (9)$$

The modeled expression above fits pretty well the experimental  $I_{DS}$ - $V_{GS}$  characteristics in the linear domain as shown in figure 5 for  $V_{DS}=0.1V$  and  $V_{DS}=0.4V$ . A small discrepancy is observed for  $V_{DS}=0.1V$  since the model assumes a zero transconductance  $g_m$  at zero  $V_{DS}$ . The main benefit of such an analytical model, in addition to its simplicity, is to predict the electrical behavior of Nanoscale devices based on SOI technology and of new materials for which leakage and series resistance due to quantum effects are of major concern [20, 21].

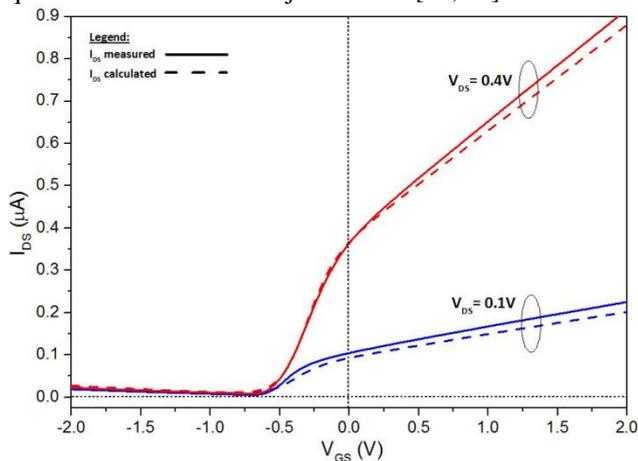


Fig.5.  $I_{DS}$ - $V_{GS}$  measured vs. calculated characteristics, using analytical Model (for the 1.6 nm thick device).

### C. Experimental Confirmation of the Series Resistance Interpretation

In order to discriminate the series resistance from the channel resistance and to eventually indicate its origin, we used the classic measured  $R_m$  -L method [22] (figure 6) coupled to the measurement of the Gate to Channel capacitance [23] (figure 7). The mobile charge density can be then extracted as function of gate voltage (figure 8) allowing an evaluation of the effective mobility  $\mu_{eff}$ . We compared results obtained for NSB (Nano-Scale Body devices, e.g. channel thinned to 1.6 nm) to those obtained for UTB (Ultra-Thin Body devices, e.g. non-thinned channel 46 nm thick for reference) at different gate lengths (L) 6 $\mu$ m, 8 $\mu$ m and 100 $\mu$ m and for different gate voltages 0V, 1V and 4V (both above the threshold voltage).

As shown in figure 6, the measured resistance  $R_m$  (reciprocal slope of the  $I_{DS}$ - $V_{DS}$  linear characteristics) for the reference UTBs exhibits a linear growth trend with L, and a decreasing trend with  $V_{GS}$  as expected from the classic MOSFET's channel resistance as given by equation (1). Since the effective mobility  $\mu_{eff}$  for UTB depends on  $V_{GS}$ , the linear  $R_m$ -L trends do not converge in a single

value at zero L, so the series resistance  $R_{SD}$  cannot be evaluated accurately by extrapolation, but the order of magnitude is found low enough (about 10  $\Omega$ ) to be compatible with conventional MOSFET contacted with doped poly silicon. This series resistance includes also the resistance of the silicon extensions regions (46 nm thick and 6  $\mu$ m length as seen in figure 3) from the Source (or Drain) contact edge to the channel edge which is constant with L.

However, for NSBs, the huge  $R_m$  values (about 1 M $\Omega$ ) remain almost constant with L and only decrease with  $V_{GS}$  as modeled by equation (5). These observed trends were confirmed for both UTBs and NSBs by using the Y-Function-based method [24] (not presented here). Therefore, these results indicate that the NSB resistance is not related to the intrinsic channel resistance but is apparently "pinned" by an external series resistance that is almost independent of L. We suggest relating this series resistance to the "bottlenecks" of the source and drain extensions near the channel. As seen in figure 3, the nitride layer is folded by the thinning process in these areas and then may induce a compressive strain that pinch the "bottlenecks". However, the influence of the strain on the transport properties of the device is beyond the scope of the present paper.

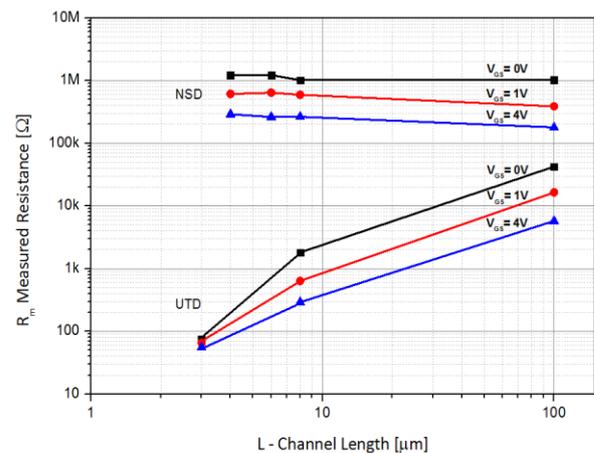


Fig.6. Measured Resistance  $R_m$  for NSB and UTB versus Channel Length (L) for several  $V_{GS}$  values. Unlike UTBs, the graph demonstrates that for NSBs there is almost no influence of the Channel Length.

In order to investigate the contribution of the inversion layer of the channel to the electrical conduction of the NSB, the Gate-to-Channel capacitance ( $C_{GC}$ ) were measured vs.  $V_{GS}$  and compared to UTB for two frequencies (100 kHz and 1 MHz). The results are compared to those obtained for UTB. In this set-up, the Drain and Source contacts are connected together while the substrate contact is grounded. As presented in figure 7, it clearly appears that below the threshold voltage  $V_T$  (about -0.5V) the UTB's capacitance is limited by the non-negligible overlap (or fringing) capacitance  $2C_{ov}$  of about 4.5 pF and 3.9 pF at 1MHz and 100 kHz respectively. The overlap or fringing regions are located at the edge of the extension regions with the channel. The positive shift of

the capacitance with the frequency may be due to the influence of the cable capacitance on the offset capacitance value (significant at 1 MHz). Above  $V_T$ ,  $C_{GC}$  increases and saturates since the contribution of the channel capacitance ( $C_{CH}$ ) is increasing and gets into its strong inversion value as observed in conventional MOSFET. The similitude of the UTB curves for the both frequencies show the interface traps below the gate are not responding and are negligible for these devices.

For the NSB device having the same dimensions and below  $V_T$ ,  $C_{GC}$  is also limited by the non-negligible overlap (or fringing) capacitance  $2C_{ov}$  (both extensions regions) of about 6 pF and 7.3 pF at 1MHz and 100 kHz respectively. The small difference of  $C_{ov}$  between NSB and UTB may be due to the additional capacitance of the bottleneck region. But, surprisingly, above  $V_T$ ,  $C_{GC}$  begins to saturate up to 1V and then steeply decreases before saturating to a value lower than the initial  $2C_{ov}$  value. Moreover, the  $C_{GC}$  maximum at zero  $V_{GS}$  (contribution of the channel) decreases strongly by increasing the frequency from 100 kHz to 1 MHz. This could be explained by the presence of interface states that contribute to an additive capacitive component to  $C_{GC}$  at lower frequency[25]. These interface traps, located below the gate and at the upper silicon/silicon oxide interface may be introduced during the thinning (oxidation) step of the gate recessed process.

The mobile charge density  $Q_n$  ( $C/cm^2$ ) of the channel can be evaluated by integrating the previous curves  $C_{GC}$ - $V_{GS}$  [25] after subtracting the  $2C_{ov}$  values (to extract the channel contribution  $C_{CH}$ ) and by normalizing to the gate area ( $80\mu m \times 8\mu m$ ). In figure 8,  $Q_n$  is plotted versus  $V_{GS}$  for UTB and NSB at 100 kHz and 1 MHz. While for UTB, the mobile charge density is increasing linearly in strong inversion (above  $V_T$ ), it is decreasing steeply and vanishing for NSB. By combining  $Q_n$  with the measured conductance ( $1/R_m$ ) for a given  $V_{GS}$ , we can extract the effective mobility according [Schroder p.541]:

$$\mu_{eff} = \frac{L}{W} \cdot \frac{1}{R_m} \cdot \frac{1}{Q_n} \quad (10)$$

For UTB, the mobility values extracted from (10) are compatible with the universal mobility curve (Schroder) [25, p546] Ошибка! Закладка не определена.. However, for NSB, the effective mobility has a value of about  $1 \text{ cm}^2/Vs$  as extracted for  $V_{GS}=1V$  for which  $Q_n$  is max at 100 kHz (see figure 8). This value is a too low value compared to literature for the same kind of devices (Schmidt) [16]. Moreover, the dependence of  $\mu_{eff}$  with  $Q_n$  is not coherent at high  $V_{GS}$  values. This reveals the limitation of the mobility extraction method based on the C-V analysis in case of strong series resistance and/or mobile charge trapping. Consequently, the interpretation of the anomalously low conductance of the NSB relative to UTB may be better described by a series resistance model rather by an electron mobility model.

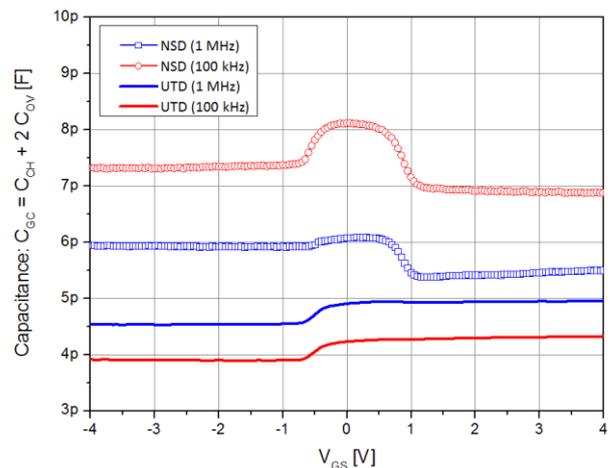


Fig.7. Representation of the  $C_{GC}$  graphs as a function of the  $V_{GS}$  voltage.

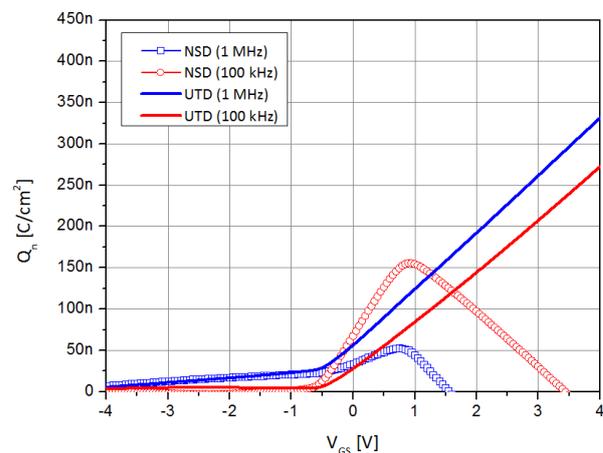


Fig.8. Representation of the  $Q_n$  graphs as a function of the  $V_{GS}$  voltage.

#### IV. DISCUSSION ON THE PROBABLE ORIGIN OF THE SERIES RESISTANCE

First of all, we can argue that the NSB series resistance could not be linked to the conventional series resistance of the drain and source regions as measured for the UTB. Indeed, since a gate recessed process was used, the source and drain extension regions remained at their original thickness, so the source and drain series resistances are not expected to be affected by the thinning process [26].

Secondly, phenomena which usually increase the spreading resistance, like the lateral gradient of source-drain dopant concentration near the silicon channel extremities [27] or a source-drain mask mismatch, are not found enough significant to explain the measured difference.

A third and significant argument may be the influence of the SOI interface quality. Indeed, Schmidt and al. [16] have measured mobility curves using UNIBOND™ SOI starting material for their samples, using a 4 points set-up and avoiding the influence of a series resistance for channel thicknesses lower than 5nm. Compared to

UNIBOND™ samples, SIMOX devices have, in general, a lower mobility and higher interface trap concentration at the upper Si/BOX interface [28]. Anyway, their carefully mobility values are still too high to explain our huge resistance values.

Finally, we suggest that the NSB resistance originate from the "bottlenecks" of the silicon extension regions with the channel that are induced by the thinning process and are not sensitive to the channel length. The  $V_{GS}$  control on  $R_m$  may due to the overlap and/or fringing capacitances of the gate with these "bottlenecks" regions which can be inverted at positive gate voltage [26]. Moreover, it appears that the inversion mobile layer become trapped under the gate at positive  $V_{GS}$  which may also contribute to increase the device resistance.

## V. CONCLUSIONS

The anomalous Transfer Characteristics of SOI MOSFET Nanoscale Devices (NSB) as thin as 1.6 nm have been analyzed and modeled by including the effects of a huge source-drain series resistance and gate current leakage. We show that the mobility extraction method based on the C-V analysis is limited in case of strong series resistance and/or mobile charge trapping. So the interpretation of the anomalously high resistance of the NSB relative to UTB is better described by a series resistance model rather by an electron mobility model. The origin of the series resistance can be related to the source-drain extensions regions and its bottleneck to the channel extremities which are not sensitive to the channel length. This generic model and investigation method may be helpful to guide Failure Analysis (FA) Modeling of FDSOI MOSFET and other Transistor-like Nanoscale Devices Regime.

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## CONFLICT OF INTEREST

The authors have no conflict of interests associated with this paper.

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