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Dual Threshold Voltage Design for Reduction of Leakage Power

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***Abstract* – Dual-Vth technique is a mature and effective method for reducing leakage power consumption. Previously proposed algorithms assign logic gates with sufficient timing slack to high threshold voltage to reduce leakage power without impact on timing. Meanwhile, clock skew scheduling algorithms are always utilized to optimize period or timing slack. In order to further reduce subthreshold leakage power consumption, in this paper, we ingeniously combine dual voltage assignment technique with intended clock skew scheduling: First, a leakage weight based clock skew scheduling algorithm is proposed to enlarge the leakage power optimization potential. Then we employ a dual-threshold voltage assignment algorithm to minimize leakage power. Three timing optimized industrial circuit blocks, among which each has around one hundred thousand gates, have also been optimized.**

***Keywords* – Low Power, Leakage, Dual-threshold, Clock Skew.**

I. INTRODUCTION

As the technology progress, leakage power has become a significant source of power consumption in integrated circuits. To reduce leakage power, several techniques have been proposed [1]. Among these techniques, dual-threshold voltage (dual-Vth) provides a low cost and effective approach. In dual-Vth designs, high-Vth gates are used on non-critical paths because they have larger delay and less leakage power while low-Vth gates are used on critical paths since they are faster at the cost of more leakage power.

Dual-Vth cell assignment techniques have been studied extensively. Several fast and effective algorithms are proposed to reduce static power caused by sub-threshold leakage current [2-7]. Most of the traditional methods implicitly assume that all flip-flops in the circuit have the same clock latency, i.e., the clock skew between flip-flops is always zero, or the clock latencies of flip-flops are constant. In [8], the method of leakage power aware clock skew scheduling is proposed. They integrate clock skew scheduling and threshold voltage assignment into one optimization formulation and use Linear Programming (LP) technique to solve this problem. The introduced clock skew sleverage on the borrowed time to achieve leakage power reduction. Compared to other methods, it can save more power dissipation.

However, LP method is not practical since it cannot solve large size problem within a reasonable time period. In order to reduce leakage power using dual-Vth in conjunction with clock skew scheduling in reasonable time, we offer a multi-step approach: First, we compute leakage weight for each adjacent flip-flop pair. Then we propose a leakage weight based clock skew scheduling algorithm to increase optimization potential. At last, under the clock latencies given in last step, dual-Vth assignment algorithm is applied to reduce leakage power.

II. EXISTED METHOD

The basic idea of leakage reduction-aware skew scheduling is to borrow slack from some non-urgent combinational blocks for better leakage power reduction in some other urgent blocks. Assuming that ∆Delay of each gate is 1ns, normal dual-Vth assignment will assign two gate in right block to High-Vth. However, it can be easily noticed that, the gate count of left block is quite larger than the number of the right one. If flip-flop vf is assigned more clock latency by 3ns, the slack of the left block will be 3ns.

First, the circuits are synthesized and timing optimized in Microwind with only low-Vth cell library for best performance. Then we extract the graph G for our circuit from micro wind Prime Time: gates are converted to nodes in graph, timing arcs between gates are converted to edges in G, the cell delay, delay increment and power information are stored in the nodes. We replace all the gates to high-Vth so the delay increment can be computed. High-level synthesis takes algorithmic descriptions as input, and outputs the register transfer-level descriptions, which shrinks the rapidly growing designer productivity gap that limits the number of transistors that can be manufactured perchip. In this paper, we propose and investigate two scheduling algorithms that can automatically generate low-leakage-power and high-performance scheduling solutions.

To make the timing analysis accurate, we consider both rising and falling delays of each gate in our algorithm since the difference between delay increments of rising and falling propagations at a single gate is comparable with cell delay.

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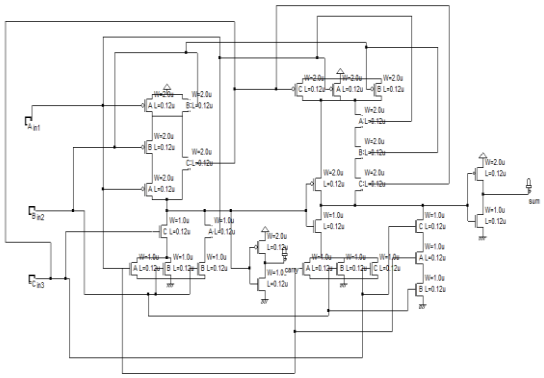


In our algorithm, for faster computing, the delay increment on a single gate does not change when its context is altered, like [3], while in fact the cell delay and delay increment could change a little since its input transition and output load capacitance may have changed during dual-Vth assignment. Thus, there may emerge very few violations after power optimization. We utilized a simple script to fix this by changing a high-Vth gate back to low-Vth, one path after another in Prime Time. The following power data are based on the results after performing dual threshold operation.

Pmos w=2(μm) Nmos w=1(μm)	
Vth(v)	**Power(μw)**
0.25	47.007
0.28	45.458
0.50	38.892
0.75	34.543
1.00	32.421

The output is shown in above figure

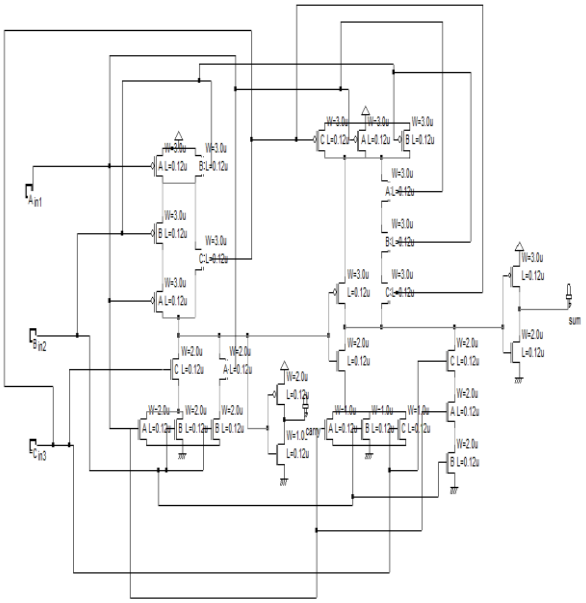
III. PROPOSED METHOD

In the previous method the output is obtained by applying single threshold voltage to the circuit. So the power consumed by the circuit is high. And now to reduce the power consumed by the full adder circuit in the existed method we are going to apply the dual-threshold voltage technique to that circuit.

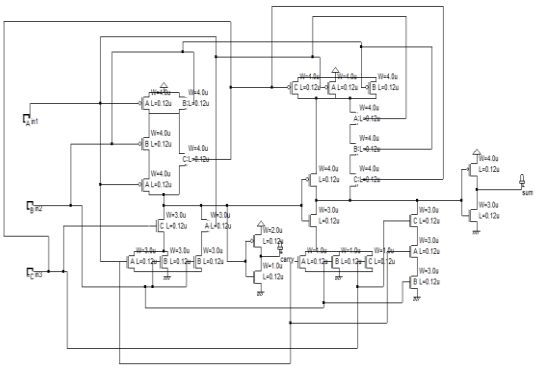
The dual-vth is applied to the circuit by the following process. For a logic circuit, a higher threshold voltage can be assigned to the transistors in off-critical paths so as to reduce the leakage power. Both high performance and low-leakage power can be simultaneously achieved with no additional transistors. Therefore, many studies apply the dual-threshold voltage (dual-*V*th) technology with gate sizing to reduce the leakage power.

In the full adder circuit the transistors that are in the off-critical path are assigned with low-vth,so as to reduce the leakage power.

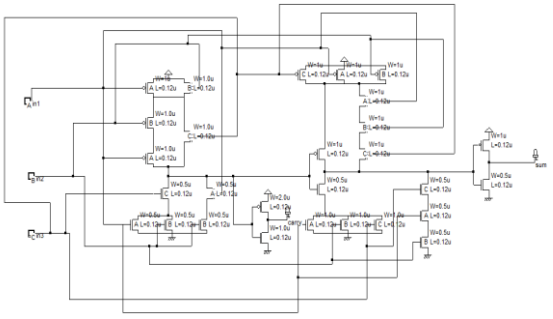
This is shown in below fig.



(a)



(b)



(c)

Fig . (a,b,c)f ull adders with different Dual-Vth designs

IV. RESULT

By using Dual-Vth technique the power of the circuit is reduce and the results are sown in the tabular column.

Pmos w=2(μm) Nmos w=1(μm)		Pmos w=1(μm) Nmos w=0.5(μm)	
Vth(v)	Power(μw)	Vth(v)	Power(μw)
0.25	47.007	0.25	30.040
0.28	45.458	0.28	28.869
0.50	38.892	0.50	23.395
0.75	34.543	0.75	20.019
1.00	32.421	1.00	18.424

V. CONCLUSION

We propose a new algorithm for leakage reduction with clock skew scheduling enhancement. The proposed leakage weight based clock skew scheduling redistributes setup slack for better leakage optimization. Compared with traditional dual threshold voltage assignment algorithm, our method can save additional leakage power up to 41.3% and 9.87% on average within only several seconds for benchmark circuits.

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