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Design of an Efficient Full Adder for Low Power Applications

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Abstract **– Adders are the key building blocks of the ALU circuit. Arithmetic and logical unit operations takes a important role in any of the systems any changes to adder circuit directly affect on the processor by using proposed system it gives very accuracy and at the same time it gives the fast of operation because we are reducing the transistors. The proposed system gives high speed with low area consumption. To overcome this drawback I have gone through different types of techniques and found the better method in terms of are power and delay are a key building block in arithmetic and logic units (ALUs) [1] and hence increasing their speed and reducing their power/energy consumption strongly affect the speed and power consumption of processors. There are many works on the subject of optimizing the speed and power of these units, which have been reported in. Obviously, it is highly desirable to achieve higher speeds a low-power/energy consumptions, which is a challenge for the designers of general purpose processors.**

Keywords **– Design, Low Power Application, Full Adder.**

I. INTRODUCTION

Complementary metal–oxide–semiconductor, abbreviated as CMOS, is a technology for constructing integrated circuits. CMOS technology is used in microprocessors, microcontrollers, static RAM, and other digital logic circuits. CMOS technology is also used for several analog circuits such as image sensors (CMOS sensor), data converters, and highly integrated transceivers for many types of communication. In 1963, while working for Fairchild Semiconductor, Frank Wan lass patented CMOS. It is also sometimes referred to as complementary-symmetry metal–oxide semiconductor (or COS-MOS). The words "complementary-symmetry" refer to the fact that the typical design style with CMOS uses complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors (MOSFETs) for logic functions. Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Since one transistor of the pair is always off, the series combination draws significant power only momentarily during switching between on and off states. Consequently, CMOS devices do not produce as much waste heat as other forms of logic, for example transistor–transistor logic (TTL) or NMOS logic, which normally have some standing current even when not changing state. CMOS also allows a high density of logic functions on a chip. It was primarily for this reason that CMOS became the most used technology to be implemented in VLSI chips.

II. EXISTED SYSTEM

A carry skip adder (CSKA) structure that has a higher speed yet lower energy consumption compared with the conventional one. The speed enhancement is achieved by applying concatenation and incriminations schemes to improve the efficiency of the conventional CSKA (Conv-CSKA) structure. In addition, instead of utilizing multiplexer logic, the proposed structure makes use of AND-OR-Invert (AOI) and OR-AND-Invert (OAI) compound gates for the skip logic. The structure may be realized with both fixed stage size and variable stage size styles, wherein the latter further improves the speed and energy parameters of the adder. Finally, a hybrid variable latency extension of the proposed structure, which lowers the power consumption without considerably impacting the speed, is presented. This extension utilizes a modified parallel structure for increasing the slack time, and hence, enabling further voltage reduction. The proposed structures are assessed by comparing their speed, power, and energy parameters with those of other adders using a 45-nm static CMOS technology for a wide range of supply voltages. The results that are obtained using HSPICE simulations reveal, on average, 44% and 38% improvements in the delay and energy, respectively, compared with those of the Conventional-CSKA. In addition, the power–delay product was the lowest among the structures considered in this paper, while its energy–delay product was almost the same as that of the Kogge–Stone parallel prefix adder with considerably smaller area and power consumption. Simulations on the proposed hybrid variable latency CSKA reveal reduction in the power consumption compared with the latest works in this field while having a reasonably high speed.

III. DESIGN OF A FULL ADDER WITH DIFFERENT LOW POWER TECHNIQUES

A. *Adiabatic Logic*

The operation of adiabatic logic gate is divided into two distinct stages: one stage is used for logic evaluation; the other stage is used to reset the gate output logic value.

1. Conventional Switching

There are three major sources of power dissipation in digital CMOS circuits those are dynamic, short circuit and leakage power dissipation. The dominant component is dynamic power dissipation and is due to charging, discharging of load capacitance.

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2. Adiabatic Switching

Adiabatic switching can be achieved by ensuring that the potential across the switching devices is kept arbitrarily small. This can be achieved by charging the capacitor from time varying voltage source or constant current source. In literature, adiabatic logic circuits classified into two types: full adiabatic and quasi or partial adiabatic circuits. Full-adiabatic circuits have no non-adiabatic loss, but they are much more complex than quasi-adiabatic circuits. Quasi-adiabatic circuits have simple architecture and power clock system.

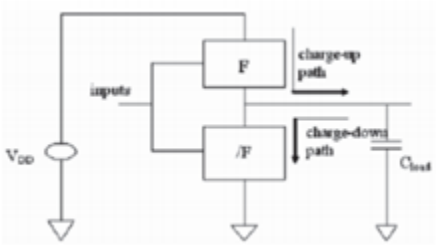

Fig: A simple Adiabatic Logic gate

There are two types of energy loss in quasi-adiabatic circuits, adiabatic loss and non-adiabatic loss. The adiabatic loss occurs when current flows through non-ideal switch, which is proportional to the frequency of the power-clock.

B. *Gate Diffusion Logic*

Gate diffusion input (GDI) - a new technique of low-power digital combinatorial circuit design - is described. This technique allows reducing power consumption, propagation delay, and area of digital circuits while maintaining low complexity of logic design. Performance comparison with traditional CMOS and various pass-transistor logic design techniques is presented. The different methods are compared with respect to the layout area, number of devices, delay, and power dissipation. Issues like technology compatibility, top-down design, and pre-computing synthesis are discussed, showing advantages and drawbacks of GDI compared to other methods. Several logic circuits have been implemented in various design styles. Their properties are discussed, simulation results are reported, and measurements of a test chip are presented.

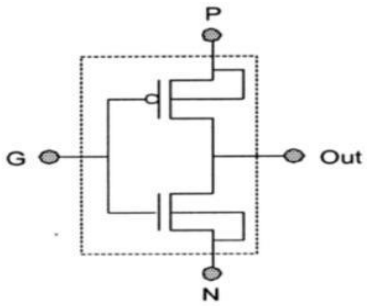

Fig: Basic GDI Cell

N	P	G	OUT	FUNCTION
'0'	B	A	A'B	F1
B	'1'	A	A'+B	F2
'1'	B	A	A+B	OR
B	'0'	A	AB	AND
C	B	A	A'B+AC	MUX
'0'	'1'	A	A'	NOT

Table: Various Logic Functions of GDI cell

IV. PROPOSED LOGIC

Pass Transistor Logic

In electronics, pass transistor logic (PTL) describes several logic families used in the design of integrated circuits. It reduces the count of transistors used to make different logic gates, by eliminating redundant transistors. Transistors are used as switches to pass logic levels between nodes of a circuit, instead of as switches connected directly to supply voltages.[1] This reduces the number of active devices, but has the disadvantage that the difference of the voltage between high and low logic levels decreases at each stage. Each transistor in series is less saturated at its output than at its input.[2] If several devices are chained in series in a logic path, a conventionally constructed gate may be required to restore the signal voltage to the full value. By contrast, conventional CMOS logic switches transistors so the output connects to one of the power supply rails, so logic voltage levels in a sequential chain do not decrease. Simulation of circuits may be required to ensure adequate performance.

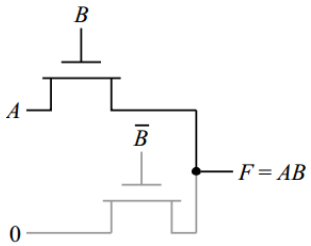

Fig. c Adiabatic AND gate

Fewer devices to implement the logical function as compared to CMOS for example take AND gate as shows in the above figure, When B is "1" top device turns ON and copies the input A to output F. When B is low, bottom device turns on and passes a "0".

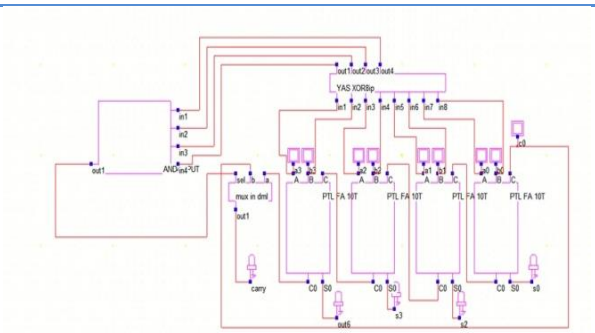

Fig. d PTL carry skip adder

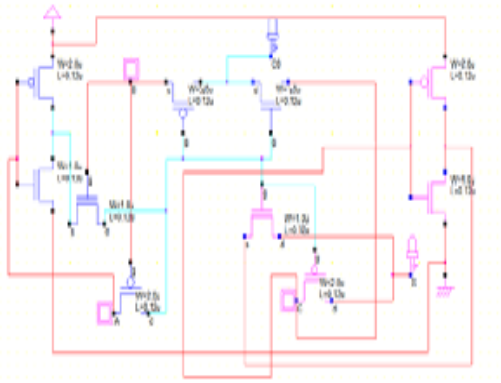

Fig. e PTL full adder

Transistor type	Power dissipation (microwatts)	Delay (nano sec)
CMOS RCA	46.67uW	3.030nS
CMOS CSKA	158.057uW	2.560nS
PTL RCA	43.55uW	1.895nS
PTL CSKA	70.uW	2.027nS

Table : A comparison of various techniques

VI. Conclusion

As in my proposed system I design a single full adder by using 10 transistor These full adders is used to create RCA and CSKA By the comparison of existed RCA/CSKA the proposed system is better in terms of Power delay and area.

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