

# Low Power Design Using Adiabatic 2:1 MUX

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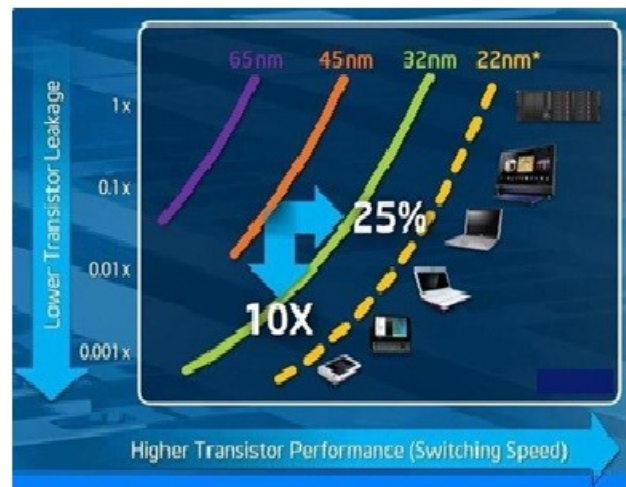
**Abstract** – A conventional CMOS logic circuit design approach depends upon charging the output capacitive nodes to the supply voltage or discharging it to the ground. This is one of the most used methods in VLSI designs. There are various techniques to design low power circuits both at system level as well as at circuit level to reduce power consumption. One of the major source of power dissipation is the charging and discharging of capacitor. Adiabatic circuits use the above two methods viz. slow charging of capacitor and discharging, and recycling of charge to minimize the power consumed. Several Adiabatic designs have been designed and tested in this paper. The technology used for simulation is 180 nm CMOS technology with 5v power supply. The input data rate for CMOS is made identical to that of adiabatic circuit. The comparison requires developing the circuit schematic based on both static CMOS and PFAL technique. Each circuit is simulated for different frequency and corresponding dynamic power is calculated through the tool Multisim V11.

**Keywords** – Adiabatic, CMOS, PFAL, ECRL.

## I. INTRODUCTION

In the last few decades due to the ever growing demand for portable and small sized devices, integrated circuits require electronic circuit design methods to implement integrated circuits with low power consumption. The ever-growing number of transistors integrated on a chip and the increasing transistor switching speed in recent decades has enabled great performance improvement in computer systems by several orders of magnitude. Unfortunately, such phenomenal performance improvements have been accompanied by an increase in power and energy dissipation of the systems. If we want a design for low-power consumption to be successful, it is important to have a thorough understanding of the sources of power dissipation, the factors that affect them and the methodologies and techniques that are available to achieve optimal results. Therefore, this thesis starts with the sources of power dissipation in a integrated circuit. We present the most important low-power methodologies and power optimization techniques available. Low -power design can be applied on various different levels, such as the architectural level, the gate level, and the technology level. Apart from that, also a number of alternative logic-design styles are presented to report on their characteristics regarding power consumption. This section could as well be utilized by others as a quick study in the field of low-power/power-aware design. Passive losses due to leakage currents are in focus with on-going shrinking of microelectronic circuits. Power-gating does not supply power to the inactive circuits from the

power supply. Uncritical paths within a complex system can be equipped with higher devices, allowing for a trade- off of speed for passive losses. Apart from these circuit level methods to reduce leakage losses also new transistor models are presented to minimize leakage losses in circuits. Each of these revolutions has been a response to challenges posed by evolving semiconductor technology. The exponential increase in the chip density drove the adoption of language - based design and synthesis, providing a dramatic increase in designer productivity. This approach held Moore's law at bay for a decade or so, but in the era of million gate designs, engineers discovered that there was a limit to how much new RTL could be written for new chip project. The result was the IP and design reuse became accepted as the only practical way to design large chips with relatively small design teams. Today even SoC design employs substantial IP in order to take advantage of the ever increasing density offered by sub-micron technology.



Moore's law

## II. METHODOLOGY

The three major sources of power dissipation in CMOS circuits is expressed using the equation given below:

$$SP \text{ Total} = P \text{ Switching} + P \text{ Short Circuit} + P \text{ Leakage}$$

$$P \text{ Total} = VVDDFCLKCLoad + ISCVDD + ILeakageVDD$$

In equation above equations, the first term represents power dissipation due to transistor switching. V is the voltage swing,

$C_{Load}$  is the load capacitance and  $F_{CLK}$  is the switching frequency of the clock. The factor  $\alpha$  is the activity factor which represents the fraction of the circuit that is switching. In most cases the voltage swing for  $V$  is almost same as the supply voltage  $V^{DD}$ , in such cases the term  $V$  is replaced with the second term in the equation represents short-circuits power dissipation which is the power dissipation in the CMOS when both PMOS and CMOS are ON simultaneously. When both transistors are ON a current value of  $I^{SC}$  flows from the supply voltage to the ground and it is known as short-circuit current  $I^{SC}$ . Apart from these two terms viz. the switching power and short-circuit power, there is always present the power loss due to leakage currents. Leakage currents depend upon various fabrication technologies related factors like threshold voltage  $V^{th}$ , device dimensions, substrate injection etc. In previous years a major contribution to the power dissipation was due to the switching but we have managed it effectively by reducing the switching frequency. Now a days the main focus is on minimization of leakage loss in the circuits, a various numbers of circuit design techniques are proposed and we are going to discuss some of them.

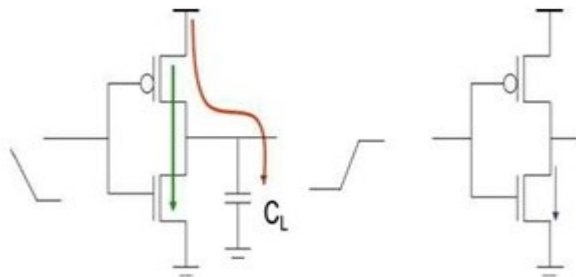


Fig.2.1 Power Dissipation

### 2.1 The Charging Process in Adiabatic Logic Compared to Static CMOS

The energy dissipation due to switching of a simple CMOS inverter as shown in Fig.1 is observed. The capacitor  $C$  at the output of the gate is the input capacitance of the following gates. Whether the PMOS or NMOS will be ON is dependent upon the input signal. If the input voltage level changes from 1 to 0, energy is transferred from the voltage source to charge the output capacitor to the supply voltage  $V^{DD}$ . A charge of  $Q=CV^{DD}$  is taken from the voltage source, an energy quantum of  $E$ .

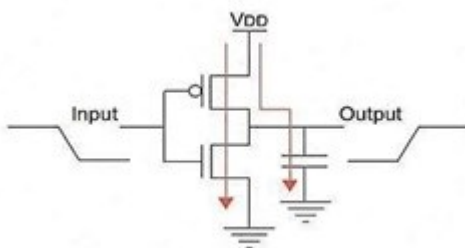


Fig. 3.2 Energy Dissipation

The energy dissipated in the circuit is equal to the

difference between the energy transferred from the sources and the energy stored in the circuit. Now if the input level changes from 0 to 1, in steady state condition the NMOS channel become ON and the PMOS is OFF. Charge stored on the output capacitance is then dissipated to the ground via the NMOS. The energy dissipation due to the switching of input level is given as

$$E_{CMOS} = 1/2 \alpha C V^{DD2}$$

Where  $\alpha$  is the switching probability of the circuit, as there is no power loss in the circuit if no switching occurs in static CMOS (except leakage losses). Different approaches are used to reduce the energy dissipation in static CMOS. Number of transistor used for a certain operation can be reduced by following different algorithm, on structural and on circuit level. Voltage supply reduction is one of the easiest and most effective method to reduce power consumption, where as it slows the performance of the circuit. "In contrast to the above method Adiabatic Logic doesn't suddenly switches from 0 to  $t$  (and vice versa), but a voltage ramp is used to charge and recover the energy from the output of the circuit.

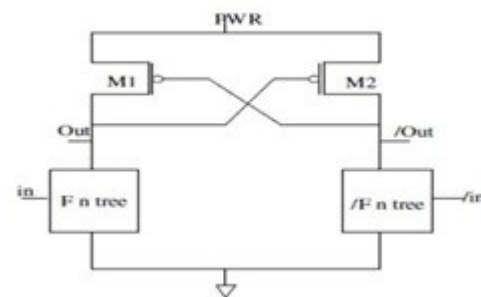


Fig. 2.3 ERCL

### 2.2 Energy Saving Factor

The energy saving factor (ESF) for a circuit can be defined as the ration between the energy dissipation by its static CMOS model and its adiabatic logic counterpart. It is a comparison of how much energy is dissipated by the static CMOS design as compared to adiabatic logic design. ESF compares the losses due to a single gate in the circuit. To calculate ESF we have to consider the supply voltage in static CMOS and power clock generation in adiabatic logic. The losses due to parasitic capacitance have also to be considered. A general definition of ESF is

$$ESF = E_{CMOS} / E_{ALL}$$

### 2.3 Low Power Design techniques

Different approaches are followed for a low power design whether It be circuit-based approach or an architectural approach, in higher level programming is used to optimize the power loss. In most of the cases a combination of these methods are used for circuit design. At the circuit level the major task is to minimize any one of the components. In the following paragraphs we have focused on different methods which are useful to minimize the losses in a design. We know that the energy required for a operation can be reduced by

decreasing the supply voltage. However due to constant threshold voltage and device capacitance the circuit performance will be slower.

#### 2.4 An Adiabatic System

Two main parts of an adiabatic system are (i) Digital core design made up of adiabatic gates and the power-clock signal generator. We have used two adiabatic families in this paper. The most important aspect of the adiabatic system is clock-signal generation. High saving factors can be achieved by an optimal generation of four-phase power-clock. Positive Feedback Adiabatic Logic (PFAL) and the other is the Efficient Charge Recovery Logic (ECRL). Both operate in the same four-phase power-clock supply. PFAL is designed by the cross coupling of two inverters, which is the latch element.

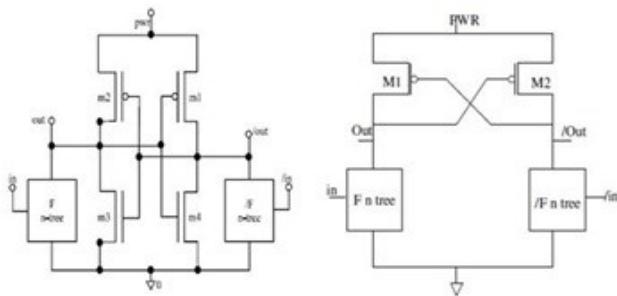
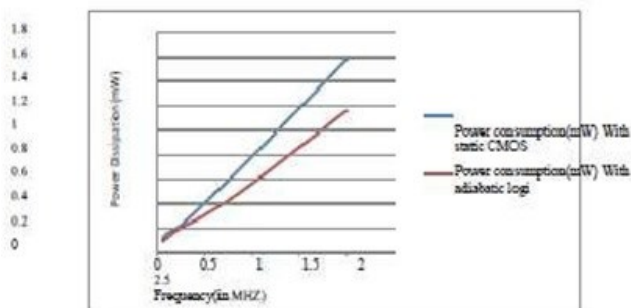


Fig.3.7 (Inverter circuits in PFAL (a) and ECRL Family

### III. RESULTS

#### 3.1 Power Comparison with Adiabatic and CMOS



by varying clock frequency

From above discussion, to compare the power dissipation with static CMOS and PFAL adiabatic logic the circuit simulation is performed using Multisim. The technology used for simulation is 180 nm CMOS technology with 5v power supply. The input data rate for CMOS 2:1 MUX is made identical to that of adiabatic circuit. The comparison requires developing the circuit schematic based on both static CMOS and PFAL technique. Each circuit is simulated for different frequency and corresponding dynamic power is calculated through the tool Multisim V11.

### IV. CONCLUSION

The main idea of this project is to introduce the design of high performance and power efficient full adder design using multiplexer based pass transistor logic. In the current work, the full adder design is implemented by different logics like SERF, PFAL, and ECRL etc. Further the design is implemented using pass transistor logic combined with other logic. The number of transistors required for realizing mixed CMOS design of full adder is less than the number of transistors required in realizing the design of full adder using CMOS transistors independently. So, the required logic can be realized within an optimized area which performs faster when compared to the conventional static CMOS full adder design.

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