

Parametric Optimization of Non Overlapped Clock Pulse Shift Register Design

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Abstract – This paper discusses the area and power optimization of shift register. The shift register is design using edge triggered flip flops. The use of latch in shift register creates timing problems which can be avoided by using pulse clock base latches as a basic cell in shift register. This resolve the timing problem created in shift register by using several non overlapping clock in a duration of pulses. This also reduces the number of cells which in turn reduces area of circuit. The shift register cell CMOS layout is design using 50nm technology in MICROWIND layout simulator tool.

Keywords – CMOS, Pulse Latch, Power Dissipation, Area Optimization.

I. INTRODUCTION

A shift register is the essential building block in a digital integrated circuit. Shift registers are normally used in many applications, such as microprocessor, microcontroller, memory design, communication receivers, and image processing ICs.

The circuit of a shift register is somewhat simple. A string of N number of flip flop base shift register is synchronized with a common clock. The speed of the flip-flop is not as much essential than the area and power consumption because there is no combinational logic between series connected flip-flops in the shift register. The smallest flip-flop is appropriate for the shift register to optimize the area and power dissipation. In recent times, pulsed latches are use instead of flip-flops in many applications, because of less number of transistors required in pulsed latch as compare with a flip-flop. But the pulsed latch cannot be used in a shift register due to the timing problem between pulsed latches. This problem is avoided by using non overlap clock pulses.

II. RELATED WORK

The area and power consumption of shift register are optimizes by using clock pulse latch instate of flip-flops in design [1]. The shift register is design by series connected clock pulse latches in a group. The several such groups of sub shift registers along with clock pulse generator. This circuit avoids the timing problems of conventional shift register. In [1] a 256-bit shift register using pulsed latches was fabricated using a 0.18 CMOS process with. The core area is the power consumption is 1.2 mW at a 100 MHz clock frequency. The proposed shift register saves 37% area and 44% power compared to the conventional shift register with flip-flops [1].

In [2] a Low power clock-gated synchronous counter using Logical Effort (LE) optimized Transmission-gate

Master- Slave Flip-Flop (TGMS FF) is proposed. Logical Effort is the transistor width optimization methodology for providing a tradeoff between area, delay and power. Logical Effort theory is the manual method for optimizing the transistor width. Out of all logic circuits, Inverter is said to be a best driver. Even a simple NAND gate will be slower than a inverter because of its topology. Hence Logical Effort uses inverter as a reference circuit and compares the driving capabilities of given gate with it [2].

In [3] a adaptive coupled flip flop circuit is use for power dissipation optimization.

In [4] Flip flop and latch designs include many timing element that are not on the critical path and this timing slack can be exploited by sing slower, lower energy TEs. Instead of simultaneously optimizing for delay and energy, critical TEs should be optimized to reduce delay and noncritical TEs should be optimized to reduce energy. Design results shows energy reduction of 63% with no loss in performance compared to a high-performance design with homogeneous flip-flop and latch structures. Compared to a design which uses transistor sizing alone to reduce energy, activity-sensitive selection results in a further total TE energy reduction of 46% [4].

III. ARCHITECTURE OF PULSE LATCH SHIFT REGISTER

This register requires 256 latches comprises of 512 transmission gates and 768 NOT logic gates. The total number of transistors for this design is 2890 for shift register chain.. The operations of the other sub shift registers are the same as that of the sub shift register1 except that the first latch receives data from the temporary storage latch in the previous sub shift register.

The 256 bit shift register is divided into sub shifter registers to reduce the number of delayed pulsed clock signals. A 4-bit sub shifter register array is synchronized through the parallel connected clock pulses through clock generator. That is clock0 is connected to the first latch of each array. Similarly the clock1, clock2 and clock3 are connected to second, third and fourth latch of each sub shift register array. When 256 bit shift register is divided into 4 bit sub shift registers, the number of clock-pulse circuits is of 4 bit and the number of latches is 256. A sub shift register consisting of 4 latches requires pulsed clock signals. Each sub shift register has a temporary storage latch [1].

IV. DESIGN RULES OF 50 NM TECHNOLOGY

Design rules are define in term of parameter λ or represent in absolute dimensions i.e. in μm . The rules are

use in such a way that the design can be easily adopted over a cross section of industrial process, making the layout portable. The scaling of lambda parameter is easily possible by changing the values. Some of the rules use in design process for 50 nano meter technology is shown below.

Design rules and electrical parameters												
Layer	Width	Spacing	Surface	Surf cap	Lin cape	Clk cape	Res	Unselci	Thickn	Height	Permitt	
	lambda	lambda	lambda	at/um ²	at/um	at/um	ohm	ohm	um	um		
nitride	0	0	0									
passiv	800	800	0									
metal6	8	15	128	30.00	25.00	12.00	0.10/sq	1.00/sq	0.50	4.00	3.00	
via5	5	5	0				1.00/via		0.50	3.65	4.00	
metal5	8	15	32	30.00	20.00	12.00	0.20/sq	1.00/sq	0.35	3.30	3.00	
via4	3	4	0				1.00/via		0.50	2.95	4.00	
metal4	3	4	32	30.00	20.00	12.00	0.20/sq	1.00/sq	0.35	2.60	3.00	
via3	3	4	0				2.00/via		0.50	2.25	4.00	
metal3	3	4	32	30.00	20.00	12.00	0.20/sq	1.00/sq	0.35	1.90	3.00	
via2	3	4	0				2.00/via		0.50	1.55	4.00	
metal2	3	4	32	30.00	20.00	12.00	0.20/sq	1.00/sq	0.35	1.20	3.00	
via	3	4	0				1.00/via		0.50	0.85	4.00	
metal	3	4	32	28.00	42.00	10.00	0.20/sq	1.00/sq	0.35	0.50	3.00	
poly	2	3	8	80.00			4.00/sq	40.00/sq	0.10	0.15	4.00	
poly2	2	2	8				4.00/sq	1.00/sq	0.00	1.00	4.00	
contact	2	3	0				2.00/via		0.50	0.00	4.00	
diffn	4	4	24	350.00	100.00		25.00/sq	250.00/s	0.10	0.00	4.00	
diffp	4	4	24	300.00	100.00		30.00/sq	300.00/s	0.10	0.00	4.00	
nwell	10	11	144	250.00			120.00/s		0.50	0.00	4.00	
oxyde				4600.00					1.80nm (4.00nm)	4.00		

Fig. 1. CMOS Layout Design Rules for 50 nm Technology

V. EIGHT BIT PULSE LATCH SHIFT REGISTER

The eight bit pulse latch shift register is design with eight latch cascaded and synchronized with four clock pulses generated from pulse clock generator. The two subgroup is design with four latch in each group. The first clock pulse of clock generator is connected to first latch of both group. Similarly the second, third and fourth clock pulse is connected to the second, third and fourth latch of both sub group. Fig. 2 shows the schematic diagram for eight bit PSR. The output of last latch in first subgroup is connected to the input terminal of first latch of second subgroup. Fig 2 shows the clock pulses connection with subgroup latches.

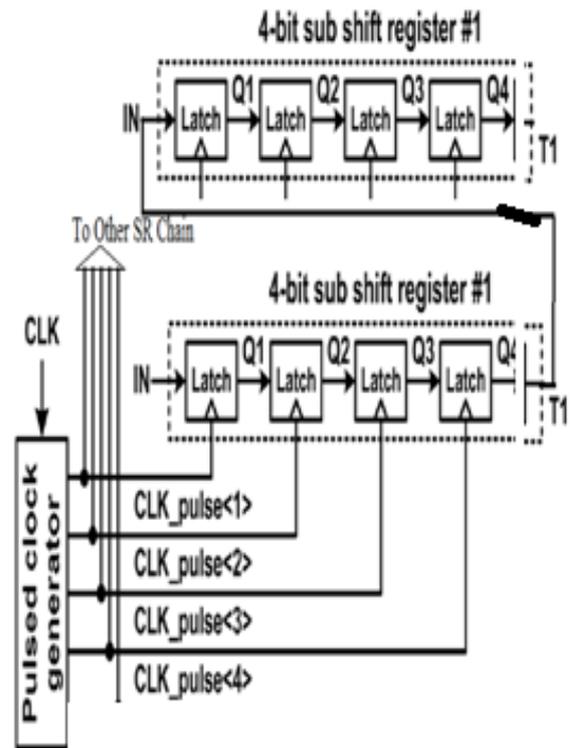


Fig. 2. Schematic Diagram for 8 bit pulse latch base shift register

The data input is shifted from first latch to its successive latches on the arrival of non-overlap pulse clocks. The latches are initial reset to logic '0' levels on arrival of reset signal. The output of each latch follows the input data on each positive level of clock pulses [1,2,3].

Two Hundred and Fifty Six bit Pulse latch shift Register

The fig shows the clock pulse shift register for 256 bit data bits. The design consist of 64 sub group of four latch each is connected in cascaded form to reduce the number of delayed pulsed clock signals. This design of 256 bit register is exactly similar to that of 8, 16 and 32 bit pulse shift register architecture. A 256 array chain of comprises of 64 sub group of 4 latch each is connected to the four non-overlap delayed clock pulses, these are clk0, clk1, clk 2, clk3. In the 4-bit sub shift register1, four latches store 4-bit data (Q1-Q4) and by the same way the clock pulses are connected to the other 63 sub group of latches.

This register requires 256 latches comprises of 512 transmission gates and 768 NOT logic gates. The total number of transistors for this design is 2890 for shift register chain. The operations of the other sub shift registers are the same as that of the sub shift register1 except that the first latch receives data from the temporary storage latch in the previous sub shift register [1,2].

VI. TIMING SIMULATION

The use of multiple non-overlap delayed pulsed clock signals as shown in Fig 4. The delayed pulsed clock signals are generated when a pulsed clock signal goes through pulse clock generator circuit. Each latch uses a pulsed clock signal which is delayed from the pulsed clock generator output signal. Therefore, each latch updates the data after its next latch updates the data. As a result, each latch has a constant input during its clock pulse and no timing problem occurs between latches. However, this solution also requires many delay circuits.

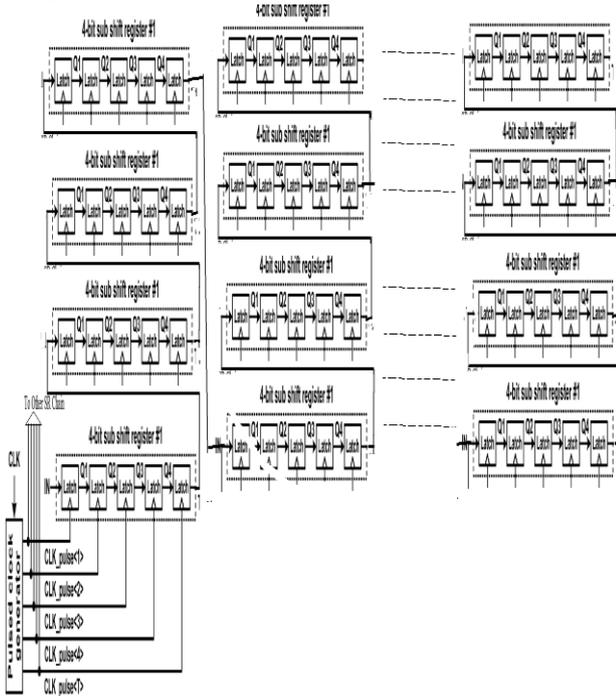


Fig. 3. Schematic Diagram for 256 bit pulse latch base shift register

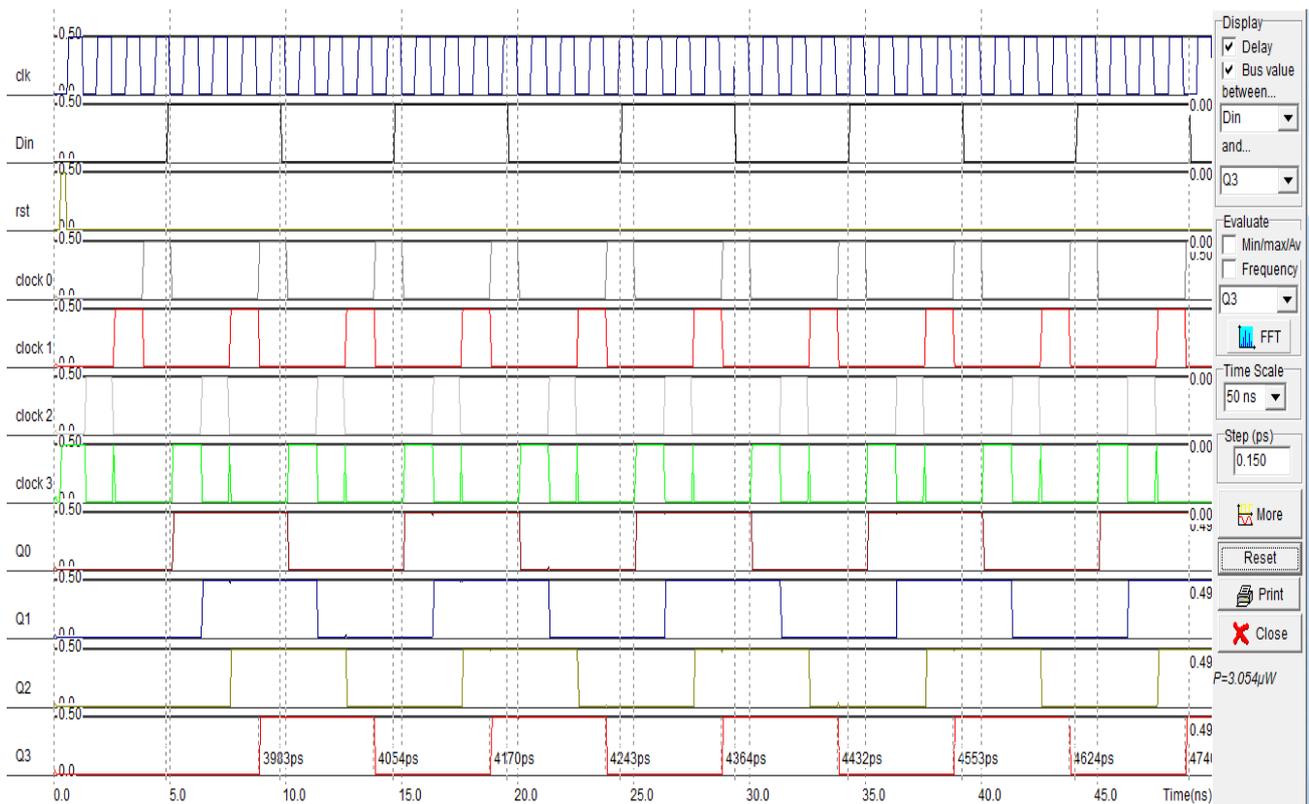


Fig. 4. Timing wave of Shift register with latches and a pulsed clock signal.

Fig. 4. shows the timing simulation of pulse clock shift register. The clock generator generates clock pulses after every 3.7 nano second which is connected to the clock signal of every individual latch. These are the non overlap

pulses. The input data at Din terminal is shifted to each flip flop after every level triggered of latches [1,4].

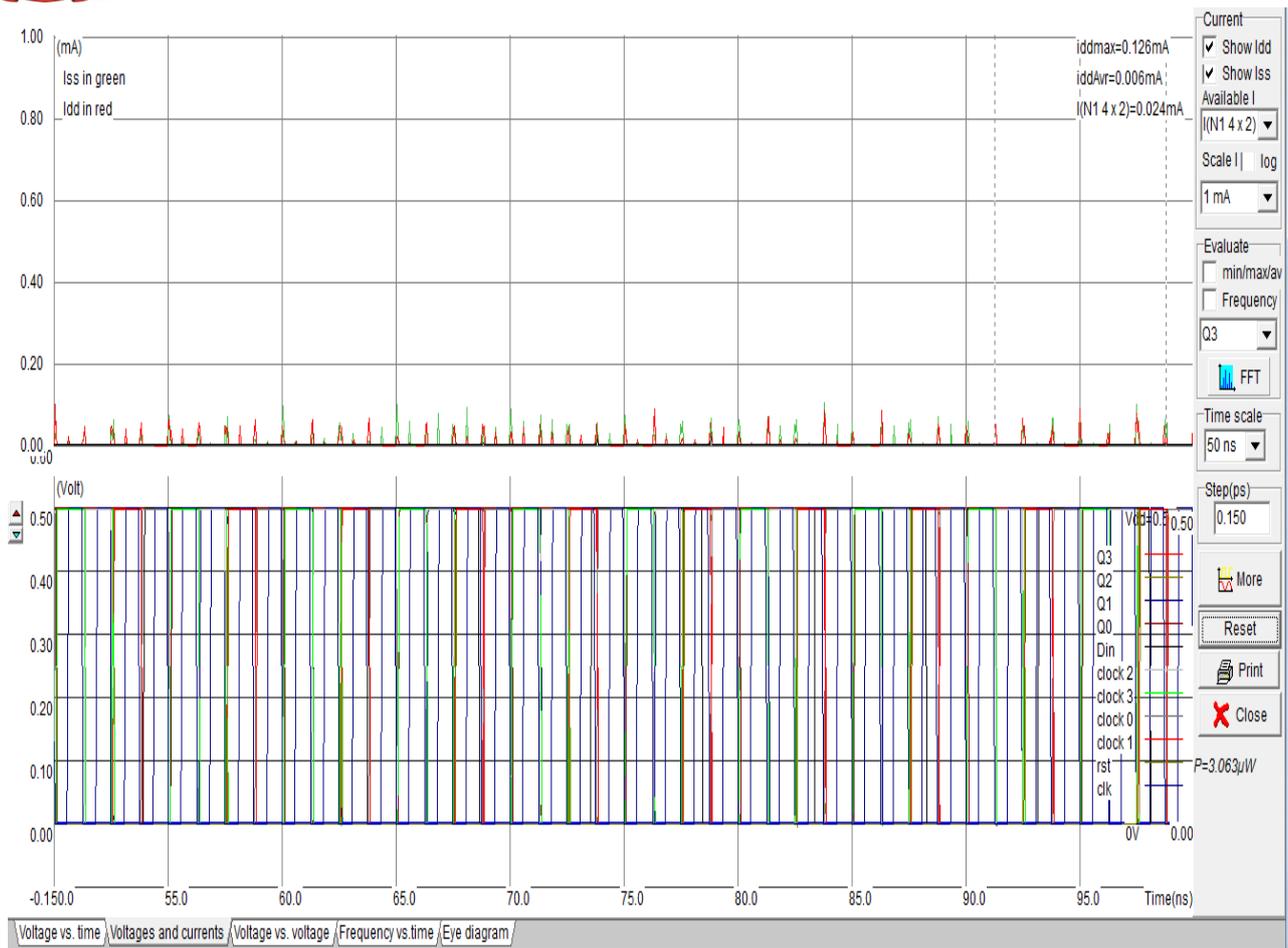


Fig 5 Timing Simulation of Voltage versus Drain to Source Current of Shift register with latches and a pulsed clock signal.

VII. CONCLUSION

The shift register is design using edge triggered flip flops. The use of latch in shift register creates timing problems which can be avoided by using pulse clock base latches as a basic cell in shift register This work discusses the schematic design and its CMOS layout implementation with optimized area and power of pulse latch base shift register. A small number of the pulsed clock signals is used by grouping the latches to several sub shifter registers and using additional pulse clock generator logic. The simulation analysis shows that the area of latch using 50nm technology is $2.8125 \mu\text{m}^2$. The power dissipation for 256 bit length shift register is computed as $41.3 \mu\text{W}$ with the area of $3162 \mu\text{m}^2$. The use of transmission gate not only reduces the number of transistors but also optimized the power dissipation of design. The timing problem of pulse latch base shift register is resolve by using the non overlap clock pulses. These pulses are generated from clock pulse generator. These latches are synchronized through non overlapped clock pulses instead of synchronized clock signal. This solves the timing problems amongst the latch base shift register design. A 256 bit pulse clock shift register requires 256 latches and a four clock pulse generator design.

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