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Reducing Power, Leakage of Standard-Cell Design using Stack Transistor Logic Design

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Abstract **– In this paper, a low leakage power optimizes CMOS layout designs. The approach is base on series-connected stack transistor technique. At first, the basic logic gate with conventional CMOS design and stack transistor base logic gate design is discussed. In stack technique, a two reduce size transistors are series connected with both gate terminals are interconnected to form single input.**

Keywords **– Stack Transistor, MOS, Transmission Gate, Layout Design, Leakage Power.**

I. INTRODUCTION

In modern design practices and tools many power reducing techniques are used which includes logic synthesis and restructuring to reduce switching activity, gate sizing, technology mapping, retiming, voltage scaling, and so on. In the same way, the variable supply and threshold voltages, body biasing, clock and power gating, transistor stacking, and so on are some of the well-known ways to reduce the power due to leakage. Out of which the stack transistor technique is the logic and circuit levels method. In a sleep transistor technique, it cuts the terminals at Vdd and/or GND connections of transistors to save leakage power consumption. On the other hand, when transistors are in standoff mode, the circuit may have to wait for a long time to reliably restore lost state and thus may affect the performance of a circuit. Therefore, retaining state is essential for systems that need fast response even while in a standby state. In stack transistor technique leakage is to force a non-stack device to a stack of two devices without affecting the input load. The stacking of two off devices has significantly reduced sub-threshold leakage compared to a single off device.

II. RELATED WORK

In [1] work on leakage power reduction with variable threshold voltage / Stack transistor, body effect method gives better results. In [2] the transmission gate and gate replacement technique to reduce the leakage power. In their technique, it adds a TG and a pullup transistor in front of the gate that needs protection with original circuit. Gates G1 and G2 are on the critical path, whereas G3 is not. During the standby mode, the output value of G1 is zero, causing stress on G2 and increasing the delay. To reduce NBTI, a TG and a pullup pMOS transistor are inserted after G1. The value after TG becomes one when the sleep signal is one, reducing the NBTI degradation. Simultaneously, gate G3 connects to the G1's output, which has a signal of zero, reducing leakage power. In [3] delay models which take the effects of the process variability and of the transient variation of the transistors' on-current during the switching into account. CMOS technology scaling enhances the computing capability of integrated circuits. Changing the substrate voltage causes the threshold voltage to change. So the different kind of effect arises for changing the substrate voltage like Zero-Body Bias, Reverse-Body Bias, and Forward-Body Bias. In [4] design a very simple series resistance extraction procedure which is derived only from the ratio of two linear ID–VG measurements. This approach has a verifiable accuracy check and is successfully used to extract the series resistance from several advanced devices. Parasitic resistance such as channel resistance (Rchannel), series resistance (R_{SD}) has become a serious obstacle inhibiting the performance of CMOS devices. As channel length scaling continues to reduce the channel resistance (Rchannel), series resistance (R_{SD}) is becoming a larger fraction of the total device resistance ($R_{Total} = R_{SD} + R_{channel}$).

III. STACK TRANSISTOR SCHEMATIC DESIGN

Power dissipation in VLSI circuits can be broadly divided into two categories: Dynamic or switching power, and Static or leakage power dissipations. Dynamic power dissipation results due to charging and discharging of internal capacitances in the circuit. Leakage power dissipation occurs during the static input state of the device. Leakage power dissipation is much more noticeable in low threshold voltage MOS transistors. This power dissipation arises because of the presence of sub threshold and gate oxide leakage currents. Subthershold leakage current flowing through a stack of series-connected transistors reduces when more than one transistor in the stack is turned off. A MOS transistor in the circuit is divided and stacked into two half-width size transistors. When two half size stacked MOS transistors are turned off together, induce reverse bias between them results in the reduction of the subthreshold leakage power. However, increase in the number of transistors increases the overall propagation delay of the circuit. Stacking transistor can reduce sub-threshold leakage. So it is called stacked effect. Where two or more stacked transistor is turned off together, the result can reduce the leakage power.

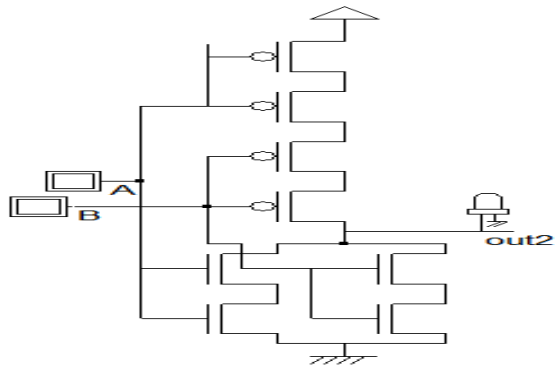

Fig. 1. Schematic Design of Stack Transistor NOR Design.

Fig 1 shows the schematic CMOS logic for stack transistor base NOR logic design. The pull up network is design by two series connected stack transistors and pull down network comprises of two parallel connected stack transistors.

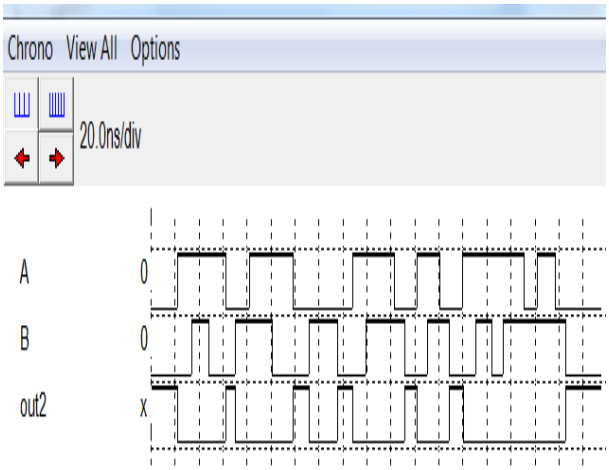

Fig. 2. Timing Simulation of Stack Transistor NOR Design.

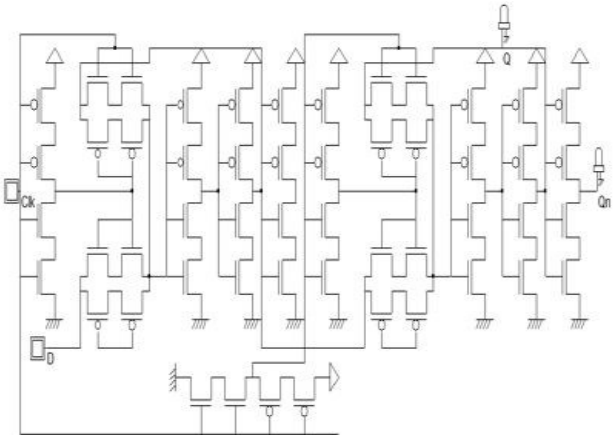

Fig. 3. Schematic Design of Stack Transistor D Flip Flop Design

Fig 3 shows the schematic CMOS logic for stack transistor base D flip-flop logic design. The flip-flop is designed using transmission gate (TG). Transmission gate base master and slave arrangement is designed with negative edge triggered clock signal.

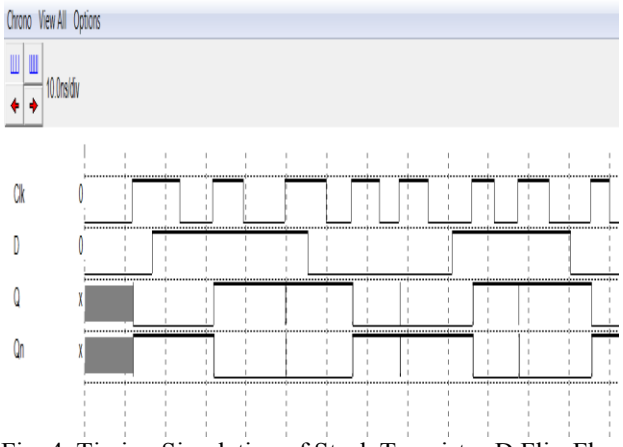

Fig. 4. Timing Simulation of Stack Transistor D Flip-Flop Design.

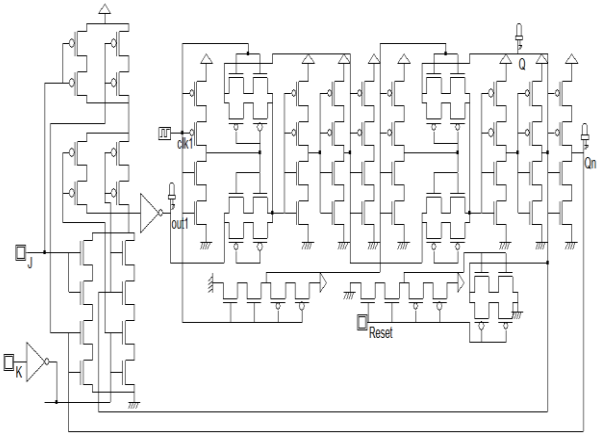

Fig. 5. Schematic Design of Stack Transistor JK Flip-Flop Design.

Fig 5 shows the schematic CMOS logic for stack transistor base JK flip-flop logic design. The flip-flop is designed using transmission gate (TG). Transmission gate base master and slave arrangement is designed with negative edge triggered clock signal. A combinational logic of JK flip-flop characteristic equation is connected at the D input terminal of D flip- flop circuit.

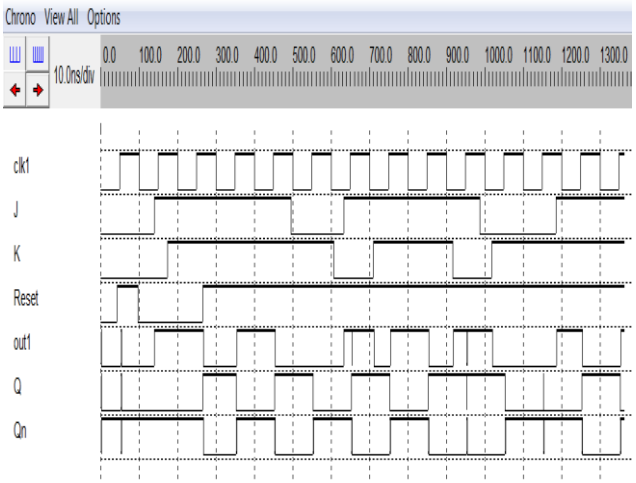

Fig. 6. Timing Simulation of Stack Transistor JK Flip Flop Design.

Delay in Series Connected MOSFET:

The saturated current flow through the MOSFET is denoted by :

$$Ids = uCox\ W/L\ \{ Vgs - Vt)^2 / 2$$

This current charge s the output load capacitor and its magnitude are constant.

The output voltage at load capacitor is

$$Vout = Ids\ t / C_L$$

Substituting this current to the output voltage, we get,

$$t = 2\ C_{L\ Vout\ /}\ uCox\ W/L\ \{ Vgs - Vt)^2$$

For the charging of load capacitor the Vgs = 0.75Vdd, Vt =1.5Vdd, Vout= Vdd,
thus

$$t = 3\ C_L / uCox\ W/L\ Vdd$$

This is the charging time of MOSFET.

Similarly for the discharging of load capacitor the Vgs = 0Vdd, Vt =1.5Vdd, Vout= 0.1Vdd, thus

$$t = 0.3\ C_L / uCox\ W/L\ Vdd$$

This is the discharging time of MOSFET.

Where,
T is switching time
C_L is Output capacitive load
U is mobility of charge carrier
Cox Is oxide capacitance
W is MOSFET channel width
L is MOSFET channel Length
Vdd is the supply voltage.

The gain and switching delay of single MOSFET is B and t respectively. If two or more MOSFET are series connected, as done in our propose work the channel length will increase. For example, if n number of MOSFETs are connected in series then the MOS transistor gain is

$$B_{series} = uCox\ W/nL$$
$$\text{i.e. } B_{series} = B/n$$

Thus the delay is estimated as:

$$t_{series} = 3\ C_L / uCox\ W/nL\ Vdd$$
$$t_{series} = nt$$

Thus the delay in series connected MOSFET is increased by the factor of number of transistors. This is the major drawback of series connected MOSFET. Thus to improve the speed of MOSFET in stack transistor technique we will improve the W/l ratio.

IV. Stack Transistor Layout Design

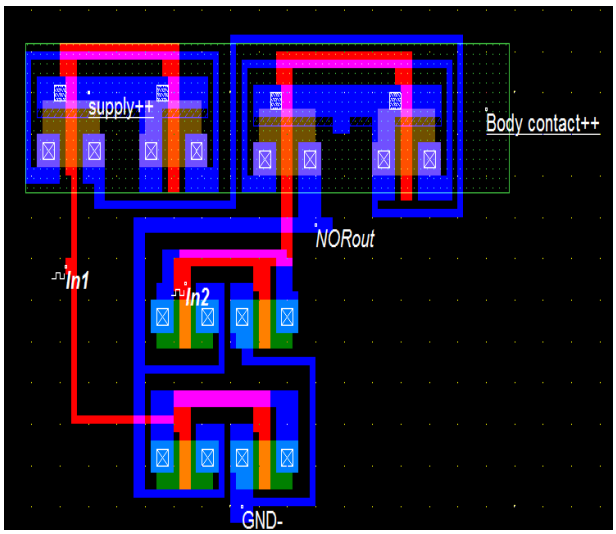

Fig. 7. Stack transistor NOR Logic Design

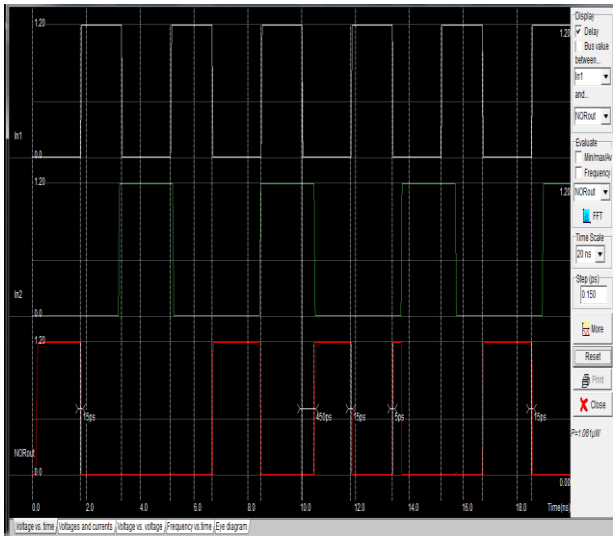

Fig. 8. Timing Simulation of Stack transistor NOR Logic Design.

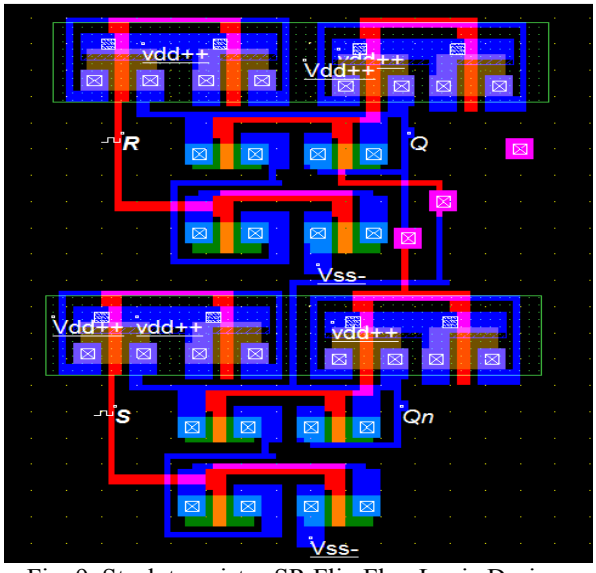

Fig. 9. Stack transistor SR Flip Flop Logic Design.

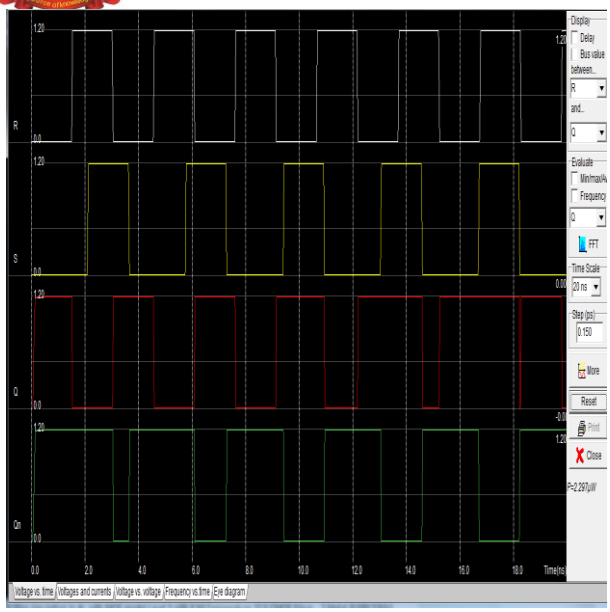

Fig. 10. Timing Simulation of Stack transistor SR Flip Flop Logic.

V. CONCLUSION

In this paper, a CMOS schematic and layout design for stack transistor technique are discussed. The stacking transistor reduces leakage power dissipation in a circuit. The stacking of two off devices has significantly reduced sub-threshold leakage compared to a single off device. Overall leakage in a stack of transistors is modelled and the opportunities for leakage reduction in the standby mode of operation are explored for scaled technologies .It is shown that, as the contribution of gate leakage relative to the total leakage increases with technology scaling, traditional techniques become ineffective in reducing overall leakage current in a circuit.

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