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Synthesis of the Output Voltage for Multilevel Inverters

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Abstract **– Trends toward large-scale integration and high-power application of green energy resources necessitate the advent of efficient power converter topologies, such as multilevel converters, with enhanced characteristics such as capability of handling voltage and power in the range of several kV and MW, respectively. For these reasons, a new family of multilevel inverters has emerged as the solution for working with higher voltage levels. Among many proposed multilevel topologies, the neutral - point - clamped, flying capacitor, and cascaded H-bridge converters are the most well-known classical multilevel topologies. To synthesize the required output voltage waveform of a multilevel inverter, different methods exist in literature. This paper investigates and analyses these methods. The most important methods are phase shifted pulse-width modulation, level-shifted pulse width modulation, and nearest level modulation technique.**

Keywords **– Modulation, Multilevel Invereters, Cascaded H-Bridge.**

I. INTRODUCTION

In recent years, industry has begun to demand higher power equipment, which now reaches the megawatt level [1, 2]. Controlled ac drives in the megawatt range are usually connected to the medium-voltage network [3, 4]. Today, it is hard to connect a single power semiconductor switch directly to medium voltage grids (2.3, 3.3, 4.16 or 6.9 kV). The inverters are used for a wide variety of applications in electrical power from component level (motor drive [5-7]) to system level (power factor correction [8]) and customer level such as direct load control in demand response applications [9-12]. The inverter topology and switching strategy have a strong impact on the total harmonic distortion (THD) for current and voltage. Having lower THD is an important factor for different applications. For example, in an electric vehicle lower current THD leads to less torque ripple [13] and as a result more convenient for the passengers. Also, electrical vehicles and renewable energy sources are an important option for future power demand due to an increased concern for the environment [14, 15]. Trends toward large-scale integration and high-power application of green energy resources necessitate the advent of efficient power converter topologies [16]. The common converter used in connecting renewable energy resources to the power grids is voltage sourced converter [17, 18] and there are other topologies such as multilevel converters, with enhanced characteristics such as capability of handling voltage and power in the range of several kV and MW, respectively [19]. For these reasons, a new family of multilevel inverters has emerged as the solution for working with higher voltage levels [20-23].

Different topologies for multilevel converters have been proposed so far in research papers [24]. Among many proposed multilevel topologies, the neutral-point-clamped [25], flying capacitor [26], and cascaded H-bridge converters [27-29] are the most well-known classical multilevel topologies, shown in Figs. 1-3. Modular multilevel inverter is another topology which has recently become increasingly popular due to its modularity and no need for dc sources [30, 31]. Fig. 4 shows a typical modular multilevel inverter.

To synthesize the required output voltage waveform of a multilevel inverter, different methods exist in literature [32]. This paper investigates and analyses in-depth these methods. The most important methods are phase shifted pulse-width modulation, level-shifted pulse width modulation, and nearest level modulation technique. Section II through IV discusses these popular modulation methods. Section V illustrates the simulation part.

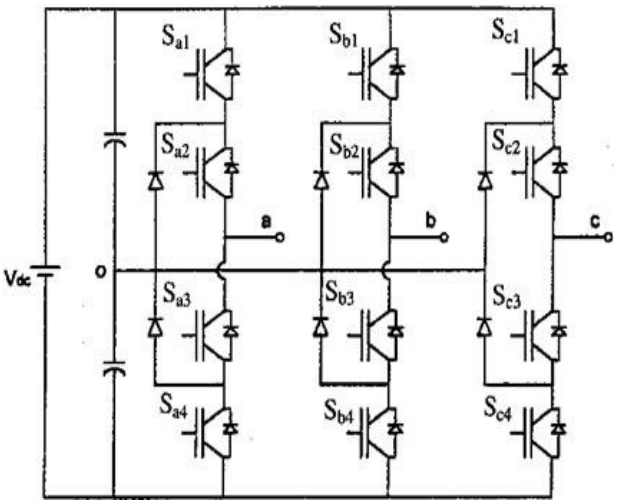

Fig. 1. Three-phase neutral-point-clamped converter

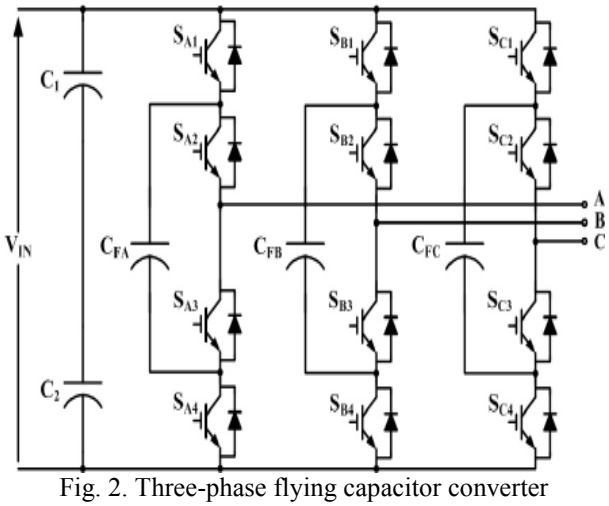

Fig. 2. Three-phase flying capacitor converter

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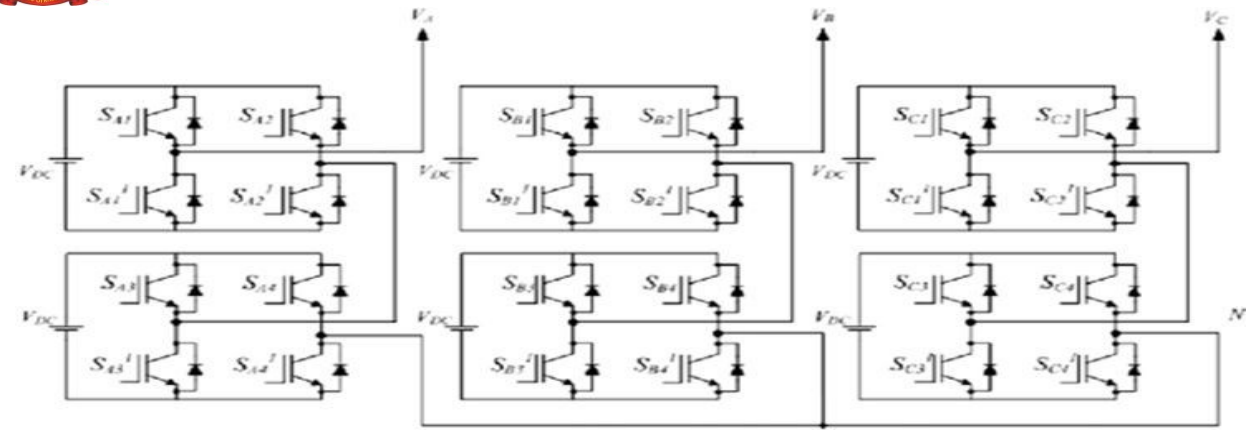

Fig. 3. Three-phase cascaded H-bridge converters

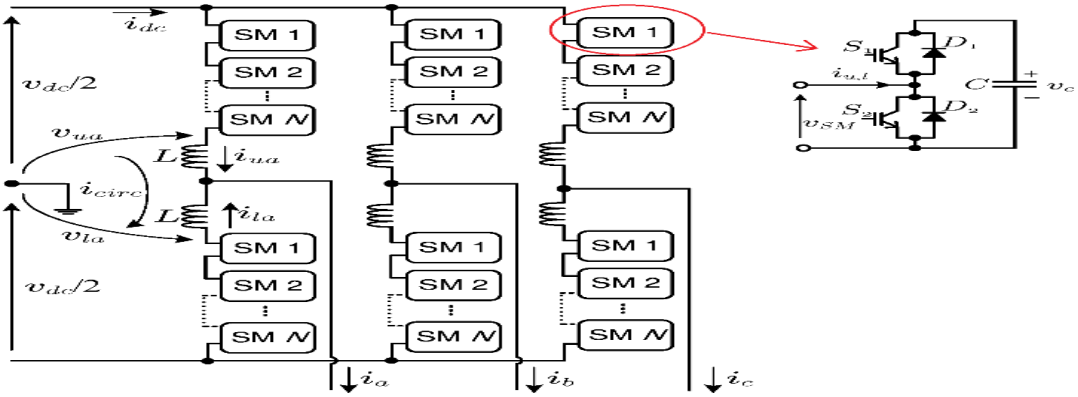

Fig. 4. Three-phase modular multilevel converters

II. Phase Shifted Pulse Width Modulation

Phase shifted pulse width modulation scheme is shown in Fig. 5. Despite the two-level converters in which only one carrier signal is used, in phase shifted pulse width modulation more than one carrier signal is used to generate the multilevel voltage waveform. As shown in Fig. 5, the control signal and the associated carrier signals are normalized between -1 and 1. The control signal is considered as sinusoidal waveform which can be the output voltage of the phase *a* of a multilevel converter. The control signals of other phases can be considered by shifting the control signal in Fig. 5 by +120 electrical degree and -120 electrical degree

In Fig. 5 it is assumed there are 8 cells in each phase of the multilevel converter. Hence, 8 equally phase shifted carrier signals have been used. Actually, each carrier is associated with one cell. By comparing the control signal with the carrier signal, the associated gating signal will be sent to the power switches in the cell. If the number of carriers in each phase is equal to *Nc*, then the required phase shift between two adjacent carrier will be obtained as:

$$\theta = \frac{360}{N_c} \qquad (1)$$

As can be seen in Fig. 5, 6 different carrier signals have been used for phase shift modulation. The angle between two adjacent carrier signals is equal to 60 degree according to Eqn. (1). Hence, these six carrier signal will span the whole 360 degree.

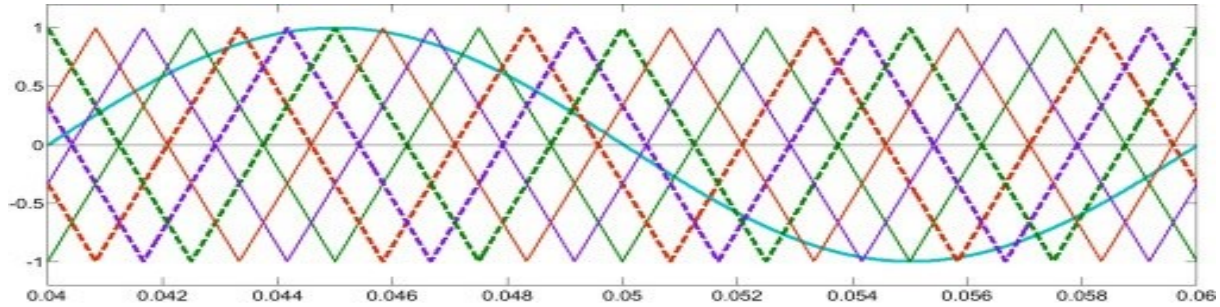

Fig. 5. Phase shifted pulse width modulation scheme

III. Level Shifted Pulse Width Modulation

Level shifted pulse width modulation scheme is shown in Fig. 6. Like phase shifted pulse width modulation, in level shifted pulse width modulation more than one carrier signal is used to generate the multilevel voltage waveform. The control signal is considered as sinusoidal waveform which can be the output voltage of the phase *a* of a multilevel converter. The control signals of other phases can be considered by shifting the control signal in Fig. 6 by +120 electrical degree and -120 electrical degree. As can be seen in Fig 6, while the control signal is normalized between -1 and 1 and the carrier signals are placed vertically covering the range from -1 and +1. Indeed the top carrier signal (in solid red) covers the range between 2/3 and +1, the next top carrier signal (the solid blue) covers the range between 1/3 and 2/3, the third top carrier signal (the solid green) covers the range from 0 to 1/3, the next carrier signal (the dashed red) covers the range from -1/3 to 0, the next carrier signal (the dashed blue) covers the range from -2/3 to -1/3, and the last carrier signal (dashed green) covers the range from -1 to -2/3.

Consider there are *Nc* cells in each phase of the multilevel inverter. Actually, each carrier is associated with one cell. By comparing the control signal with the carrier signal, the associated gating signal will be sent to the power switches in the cell. As shown in Fig. 6, while the control signal is normalized between -1 and 1, but the peak to peak value of each carrier signal, *h*, is obtained by 2/*Nc*.

$$h = \frac{2}{N_c} \tag{2}$$

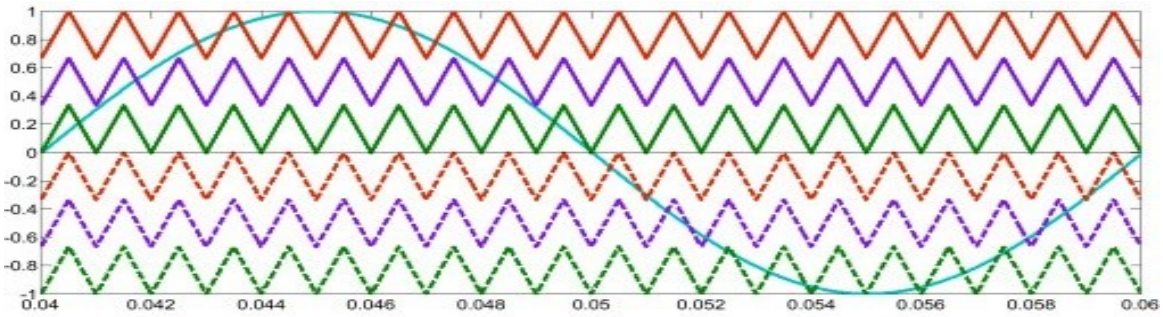

Fig. 6. Level shifted pulse width modulation scheme.

IV. Nearest Level Modulation

Nearest level modulation is very interesting solution especially when the number of employed cells in the specific multilevel inverter is quite large. For example, today there are different commercial projects with over 100 cells employed in very high voltage levels. For this case, there would be need for over 100 carrier signals with precise phase shift or level shift if phase shift modulation or level shifted modulation is supposed to be employed. But nearest level modulation avoids using carrier signals in case of large number of cells, and obtains gating signals by rounding the voltage reference. Fig. 7 shows the nearest level modulation scheme.

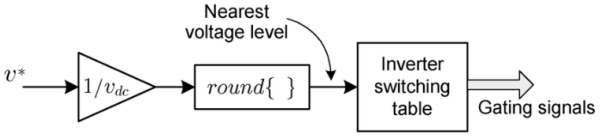

Fig. 7. Nearest level modulation scheme

V. Simulation Results

An example case has been studied in this section to show the voltage synthesis of a multilevel inverter. The multilevel inverter is chosen as the cascaded H-bridge, and the output voltage is synthesized using level-shifted pulse width modulation. The control of cascaded H-bridge is easier compared to modular multilevel inverter due to use of dc sources instead of floating capacitors. Hence there is no issue of voltage balancing for the cascaded H-bridge. To do the simulation, a single-phase 5-level cascaded H-bridge has been simulated in Matlab SIMULINK and the result is shown in Fig. 8. An R-L load of 10 ohm - 10 mH is considered. The switching frequency is set at 5 kHz. The frequency of output voltage is 50 Hz. The voltage per division of Fig. 8 is equal to 10 V. Regarding the value of the reference voltage, certain number of cells are inserted into the circuit, while the rest are bypassed. So when the reference voltage reaches to its maximum value, both of the cascaded H-bridge cells are inserted to the circuit, and output voltage of 20 V is employed on the load. This level is the top most level in the Fig. 8. As the value of the reference voltage decreases, at any moment mostly one cell is inserted in circuit. After spending half a period time, the reference voltage will be around 0, hence on average no cell will be inserted into the circuit. Next, the required output voltage will be equal to -10 V, hence one cell needs to be inserted into circuit with negative voltage polarity. When the reference voltage reaches to its minimum value, both of the cascaded H-bridge cells are inserted to the circuit with negative polarity, and output voltage of -20 V is employed on the load

Fig. 9 also depicts the gating signals for the simulated cascaded H-bridge converter. The 5 gating signals has been shown from the beginning of the simulation at time t = 0 s. It can be seen the control system is not perfectly stable and the required voltage level may not be according to voltage reference. But after one or two cycle passes, then the control signal becomes within the acceptable limit and the carriers can synthesis the control signal. This can be seen clearly in Fig. 9. While at first the gating signals for all 5 cells were 1 for half cycle and 0 for the other half, then it changes between 0 and 1 states frequently. It shows this fact that now the control signal is between the acceptable limits and the carriers can shape the output voltage.

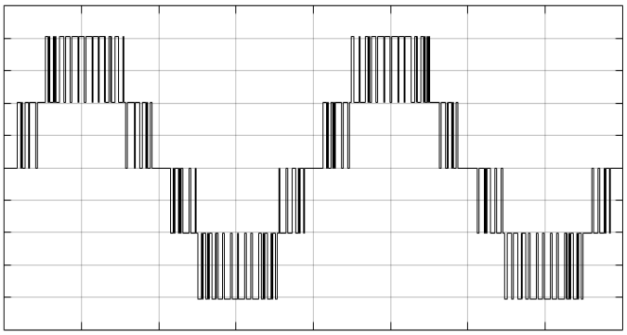

Fig. 8. Output voltage of the 5-level cascaded H-bridge multilevel inverter.

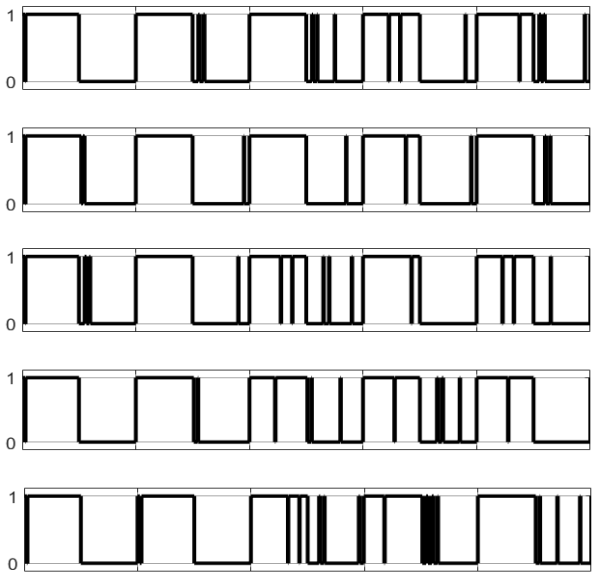

Fig. 9. Gating signals for the simulated converter

VI. Conclusion

Trends toward large-scale integration and high-power application of green energy resources necessitate the advent of efficient power converter topologies, such as multilevel converters, with enhanced characteristics such as capability of handling voltage and power in the range of several kV and MW, respectively. For these reasons, a new family of multilevel inverters has emerged as the solution for working with higher voltage levels. Among many proposed multilevel topologies, the neutral-point-clamped, flying capacitor, and cascaded H-bridge converters are the most well-known classical multilevel topologies. To synthesize the required output voltage waveform of a multilevel inverter, different methods exist in literature. This paper investigates and analyses these methods. The most important methods are phase shifted pulse-width modulation, level-shifted pulse width modulation, and nearest level modulation technique.

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