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Electrodeposited CdTe Thin Film Solar Cells: Chloride Treatment and Improved Efficiency

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Abstract **– The First Solar Company has recently reported the manufacturing cost of less than US$1 per Watt for their CdTe solar panels, achieving a major milestone in the quest for grid-parity [1]. Improving cell efficiency and reducing the processing costs will further reduce the cost of solar panels, making them viable and accessible for all. Therefore, further cost reduction requires search of low-cost growth and processing techniques to achieve similar performance. The electrodeposition technique is an attractive low cost tech--nique with proven scalability and manufacturability in the solar cell industry. Therefore in this work, initial CdTe heterojunction solar cells were fabricated by electro--deposition using a three electrode setup with an aqueous medium in order to explore and understand material issues and processing steps involved. The preliminary best deposition potential was established as 695 mV vs standard calomel electrode (SCE), and materials were characterized using X-ray diffraction, optical absorption and scanning electron microscopy. In this initial research work, complete devices were also fabricated and the best efficiency obtained to date for 2 mm x 2 mm devices was 8.4% with the open circuit voltage (V_{OC}), short circuit current density (J_{SC}) and fill factor (FF) values of 640 mV, 31 mAcm^{-2} and 0.42 respectively.**

Keywords **– Electrodeposited, CdTe, Solar Cells, Chloride Treatment, Improved Efficiency.**

I. INTRODUCTION

$CdCl_2$ treatment of CdTe layers before heat treatment is now widely used for materials grown by a variety of techniques; vacuum evaporation [2], close spaced sublimation [2] and electro deposition [2,3,4]. A key processing step is chlorine treatment which has a beneficial effect on both CdTe and CdS by passivating grain boundaries and improving crystallinity [5, 6, 7] It also promotes grain growth and decreases defect density [8]. The band gap energies of CdS and CdTe treated with chlorine have been investigated by numerous research groups and these values reach their bulk material energy gap values after $CdCl_2$ treatment. $CdCl_2$ treatment of CdS and CdTe also reduce recombination and generation process in the space charge region [9]. Various authors showed that the inclusion of chlorine ions increases the performance of CdS/CdTe solar cells parameters, with an increase in all three solar cell parameters [4, 5, 6]. Basol et al, 1986 has shown that the inclusion of Cl ions increased the J_{sc} from ~11 to 19 mA cm^{-2} for as-deposited and $CdCl_2$ treated CdTe devices respectively [4]. The effect of the inclusion of Cl ions on the performance of CdS/CdTe solar cells has been studied by Dennison 1994 [6]. It was revealed that 300 ppm background Cl ions in the electrolyte solution improved the efficiency of the CdS/CdTe device from 3 to 11%. Similarly, the effect of the inclusion of Cl on the performance of CdTe devices, has also been investigated by Barker et al 1995 [10]. It was found that 636 ppm background Cl ions in the solution gave a high efficiency of 13.5% for a CdS/CdTe device. The $CdCl_2$ treatment can be established by either deposition in an aqueous medium [5, 6, 12] with Cl ions or by dipping the CdTe layers in a $CdCl_2$/methanol solution before the annealing process [2, 11, 12, 13]. Both methods yield beneficial effects on the solar cell properties.

Experimental Aspect

The electro deposition of CdTe layers was performed from an aqueous solution containing 0.8 M cadmium sulphate ($3CdSO_4.8H_2O$) with 99% purity, 600 ppm $CdCl_2$ and 50 ppm tellurium dioxide (TeO_2) with purity of 5N (99.999%) in 800 ml deionized water. The $CdSO_4$ aqueous solution was electro-purified at a cathodic voltage of 600 mV vs SCE for 100 hours in order to remove impurities, before addition of high purity TeO_2 solution. The pH value was adjusted to 2.00 using high-purity sulphuric acid (H_2SO_4) and ammonium hydroxide $(NH)_4OH$. The temperature was maintained at 70°C throughout the experiment. The solution was stirred by a magnetic stirrer with moderate stirring rate.

CdTe films were deposited using a three electrode system, and the counter electrode was a high purity graphite rod. The reference electrode was saturated calomel electrode (SCE) with the outer jacket filled with cadmium chloride ($CdCl_2$) solution instead of potassium chloride (KCl) solution. The substrates used were glass/ FTO/n-CdS pre-prepared with CBD-CdS. The electro deposition experiments and cyclic voltammetry were carried out using a computerized GillAC V4 potentiostat/ galvanostat. The CdTe films were annealed in air atmosphere at 350ºC for 20 minutes in air. These heat treated samples are named as $CdCl_2$ treated material in this paper. Both as-deposited and $CdCl_2$ treated CdTe layers were characterised using conventional X-ray diffraction (XRD), Optical absorption and Scanning electron microscopy (SEM).

After annealing the layers in an air atmosphere, a thin oxide layer often exists on the CdTe surface depending on the growth technique. This layer acts as an insulating layer between the absorber material and the metal contact. Many experiments have been reported on wet chemical etching of CdTe material, by Dharmadasa et al [14,15]. Etching in a dilute potassium dichromate ($K_2Cr_2O_7$) solution, for 5

seconds is commonly used to oxidise the top layers further followed by rinsing in 0.1M sodium hydroxide (NaOH) plus 0.1M sodium thiosulfate ($Na_2S_2O_3$) in warm distilled H_2O to dissolve oxidised material. As soon as the etching process was completed, samples were transferred to a vacuum system to evaporate metal contacts on the layer to complete the device structures. The back electrical contacts were formed by evaporating Au through a mask with 3x3 mm^2 holes. Current-voltage characteristics were measured using a fully automated I-V system together with a AM1.5 solar simulator.

Linear Sweep Voltametry

The Linear Sweep Voltammogram (LSV) of aqueous solution containing 0.8 M $CdSO_4.8H_2O$, 600 ppm $CdCl_2$ and 50 ppm TeO_2 is illustrated in figure 1 and provides information on the material deposition taking place at different deposition potentials. The voltage scan was run between anodic 100 mV and cathodic 800 mV vs SCE with a sweep rate of 5 mVs^{-1}. Studies by Panicker et al show that Te reacts with H_2O to form $HTeO_2^+$ and become stable in the aqueous solution [16]. It can be seen from the figure that the current density starts to increase gradually from ~150 to ~500 mV because of the ease of the reduction of Te. This indicates that Te is released from $HTeO_2^+$ and deposited on the cathode. A plateau between 500 to 660 mV vs SCE is due to the diffusion-limited current attributed to the deposition of both elemental Te and CdTe compound. Beyond this voltage range, there exists a narrow voltage window which produces stoichiometric CdTe compound only. The main aim of this work is to find out this Perfect Potential for Stoichiometry (PPS), to grow device quality CdTe layers. A rapid increase in current at 660 mV vs SCE is due to an increase in Cd-deposition and hydrogen evolution at the cathode due to electrolysis of water. The reverse sweep shows a large negative current peak between 650 to 550 mV vs SCE where Cd is quickly stripped off from the cathode surface. When the potential becomes more positive, at a voltage between cathodic ~80 to anodic ~100 mV vs SCE, Te ions will be released from the sample to the solution. The result of these experiments has been used as a guide to select the potential range for the deposition of CdTe. In order to determine the perfect potential for stoichiometry (PPS), layers were grown at constant voltages beyond 600 mV, and characterised for their structural, optical and morphological properties.

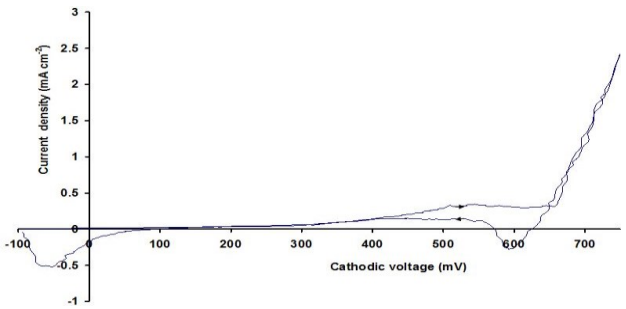


Fig. 1. Voltammogram of CdTe solution at 70°C, containing 0.8 M $CdSO_4.8H_2O$ and 50 ppm-TeO_2. The arrows indicate the direction of the potential sweep with scan rate of 5 mVs^{-1}.

II. Characterisation of Treated Cdte Material with Chlorine

X-Ray Diffraction

To identify the crystallinity and phases present in the layers, X-ray diffraction was carried out on samples deposited at different voltages. The XRD data for as-deposited and annealed CdTe layers were analysed by comparing standard data obtained from the online Deresbury Chemical Database Service [17]. Figure 2 shows the X-ray diffraction patterns of CdTe deposited at 655, 665, 675, 685 and 695 mV vs SCE. From the figures it is clear that whatever the deposition voltage, the major preferential reflection from the (111) plane is found, which was also observed by different authors [18, 19]. All materials were identified as cubic structures of CdTe, agreeing with the literature [20, 21, 22]. The patterns show a large increase in the major peak height intensity which increased as the growth voltage increased. The highest intensity peak was recorded for the layer deposited at 695 mV, whilst the lowest intensity was observed for the layer deposited at 655 mV. These changes reveal that the composition of the CdTe vary with growth voltage and crystallinity is highest at 695 mV.

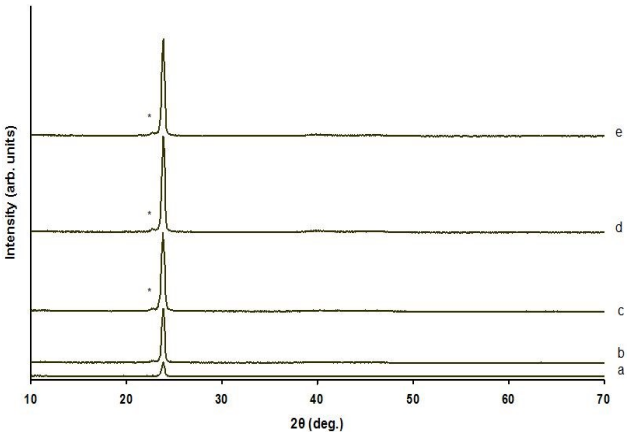


Fig. 2. Typical XRD patterns for as-deposited CdTe layers grown at: (a) 655, (b) 665, (c) 675, (d) 685 and (e) 695 mV vs SCE. The peak arising from TeO_2 or $CdTe_xO_y$ is indicated by an asterisk (*).

Figure 3. shows the variation of the (111) peak height as a function of cathodic voltage for as-deposited CdTe layers. This trend shows that the crystallinity increase as the composition reach stoichiometric value of CdTe. The peak arising on the left of (111) peak is related to TeO_2 or $CdTe_xO_y$ compounds. These compounds are in the crystalline form, most probably on the surface but any expected elemental Te in the form of amorphous phase cannot be detected using XRD technique.

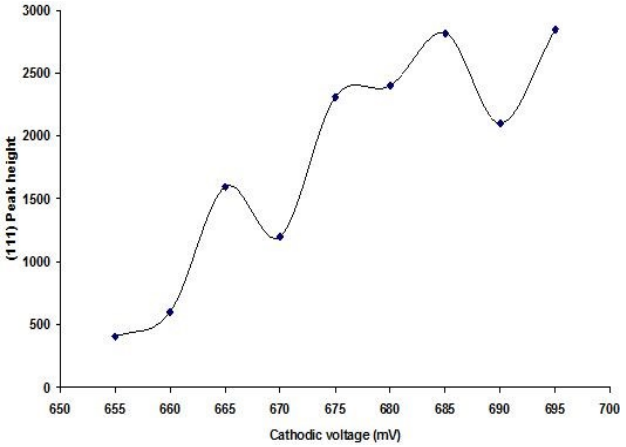


Fig. 3. Variation of the (111) peak height against cathodic voltage for as-deposited CdTe layers.

To keep the thickness of layers constant, the deposition was carried out for the same period of time. The grain size (l) was calculated using the Scherrer equation given by (2).

$$l = \frac{\lambda}{\beta Cos\theta} \qquad (2)$$

Where λ is the wavelength of incident X-rays, β is the full width at half maximum (FWHM) and θ is the centre angle of the peak. Table 1 presents peak position, FWHM and grain size as a function of growth voltage for as-deposited CdTe layers. These data shows that the values of FWHM and grain size vary with growth voltage, with the layer deposited at 695 mV vs SCE displaying the largest grain size and the smallest FWHM. Further optimisation of growth voltage is continuing but from the data to date, the 695 mV deposition provide CdTe layers with best crystallinity.

Table 1. Summary of peak position, FWHM and grain size observed as a function of deposition voltage for as-deposited CdTe layers.

Growth Voltage (mV)	2θ	FWHM (deg.)	Grain size (nm)
655	23.86	0.40	20.0
665	23.85	0.39	20.5
675	23.84	0.42	19.0
685	23.87	0.37	21.6
695	23.86	0.36	22.6

Figure 4 shows the X-ray patterns of as-deposited and annealed CdTe layers deposited at 695 mV. It is clear from the X-ray spectra that the annealed CdTe layers show larger peak intensity as compared with the as-deposited CdTe layers. This result concurs with other results reported in the literature. Abou-Elfotouh et al showed an increase in the major reflection peak from the (111) plane after $CdCl_2$ treatment of CdTe layers [23]. The annealed CdTe also shows signs of reflections from the (220) and (311) atomic planes suggesting a polycrystalline layer formation. However, these peaks suddenly appear only after heat treatment beyond 385±5ºC, as recently identified and reported in [24].

Considering the major reflection peak related to the (111) plane of annealed CdTe for layer deposited at 695 mV, a grain size of 22.6 nm with FWHM of 0.36º was estimated using the Scherrer equation. The lattice parameters were calculated using the cubic d-spacing equation (3), giving a = 6.483 Å which is very close to the standard value of a = 6.482 Å. The structural parameters are related to Miller indices (hkl) by

$$\frac{1}{d^2} = \frac{h^2 + k^2 + l^2}{a^2} \qquad (3)$$

where d is the lattice spacing (nm), and a, b, c and d (a = b = c, α = β = γ = 90°) are lattice parameters (nm).

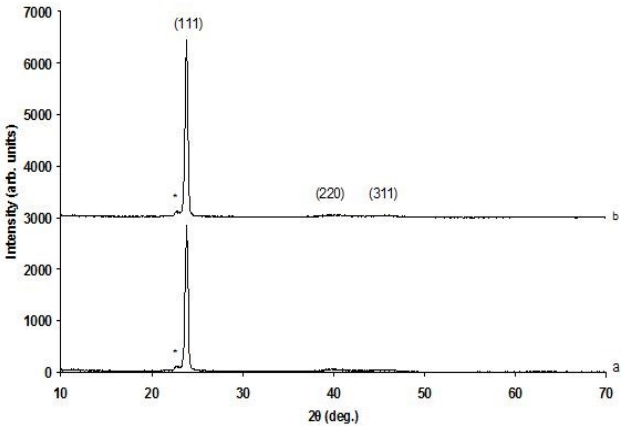


Fig. 4. The X-ray patterns of (a) as-deposited and (b) $CdCl_2$ treated CdTe grown at 695 mV. The peak arising from the TeO_2 or $CdTe_xO_y$ is indicated by an asterisk (*).

Optical Absorption

The energy bandgap of the material was estimated by measuring the optical absorption (A) as a function of wavelength and by plotting A^2 vs hν or $(\alpha h\upsilon)^2$ vs hν. Near the absorption edge, absorption coefficient (α) can be described by equation (4)

$$\alpha = \frac{k}{h\upsilon}\left(h\upsilon - E_g\right)^{\frac{n}{2}} \qquad (4)$$

where k is a constant, h is Planck's constant, E_g is energy bandgap and ν is the frequency of light. In this relationship, n = 1 for a direct bandgap semiconductor. Assuming CdTe films as single phase material (where $A \propto \alpha$), the equation can be re-arranged as shown by equation (5)

$$(\alpha h\upsilon)^2 = k'\left(h\upsilon - E_g\right) \qquad (5)$$

The influence of growth voltage on the absorption edge of CdTe layers was investigated using optical absorption with the aim of optimising the conditions for growing good quality, stoichoimetric CdTe. Figure 5 shows a plot

of absorption spectra against photon energy for as-deposited CdTe grown at different growth voltages. The CdTe was deposited on glass/FTO/CdS at 655, 665, 675, 685 and 695 mV vs SCE. A variation in bandgap between 1.52 eV and 1.57 eV was observed for these material layers. Table 2 summarises the values of band gap energy as a function of deposition voltage for as-deposited CdTe layers.

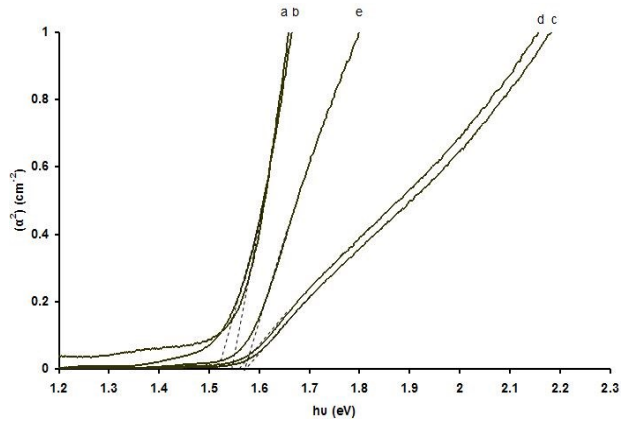


Fig. 5. Square of optical absorption vs photon energy of as-deposited CdTe for layers deposited at (a) 655, (b) 665, (c) 675, (d) 685 and (e) 695 mV vs SCE.

Figure 6 shows typical optical absorption spectra of $CdCl_2$ treated CdTe layers. The layers were deposited at 655, 665, 675, 685 and 695 mV vs SCE and annealed at 350°C for 20 minutes in air. The band gap energy of annealed CdTe layer varies between 1.46 and 1.50 eV. Farenbruch et al reported that the maximum theoretical efficiency as a function of band gap energy is in the range from 1.40 to 1.50 eV [25]. Therefore, this variation in band gap energy may affect the solar cell efficiency. The annealed layers showed lower band gap energy values as compared to as-deposited material. From the above result, the annealing of CdTe at 350°C for 20 minutes in air in the presence of chlorine is significant to obtain a band gap energy close to theoretical values. Table 2 also summarises band gap energy as a function of deposition voltage for annealed CdTe layers. The trend of optical absorption measurements show better absorption edges for layers grown at 695 mV.

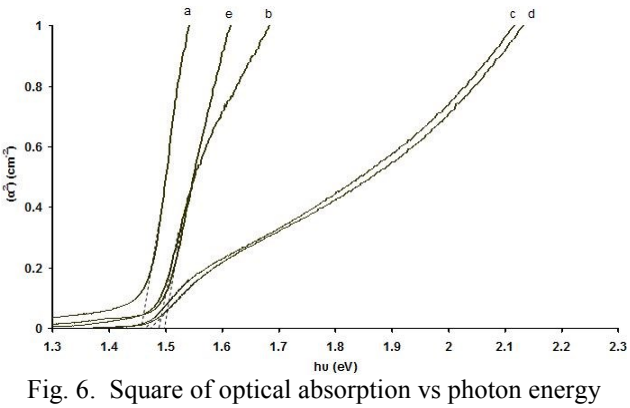


Fig. 6. Square of optical absorption vs photon energy of $CdCl_2$ treated CdTe layers deposited at: (a) 655, (b) 665, (c) 675, (d) 685 and (e) 695 mV.

Table 2. Band gap energy as a function of the growth voltage for as deposited and $CdCl_2$ treated CdTe layers.

Growth voltage vs SCE (mV)	655	665	675	685	695
Band gap energy (±0.02 eV) for as-deposited CdTe	1.52	1.54	1.57	1.56	1.57
Band gap energy (±0.02 eV) for $CdCl_2$ treated CdTe	1.46	1.49	1.46	1.47	1.50

In order to determine the transmission for as-deposited and $CdCl_2$ treated CdTe layers at different wavelengths for different growth voltages, the transmission spectra were recorded and presented in Figure 7. These results show that different growth voltages give different transmission percentages. The maximum transmission percentage of ~93% was obtained for a layer deposited at 685 mV. The minimum transmission percentage of about ~59%, was observed for a layer deposited at 655 mV. This low transmission must be due to the high level of Te present in these layers.

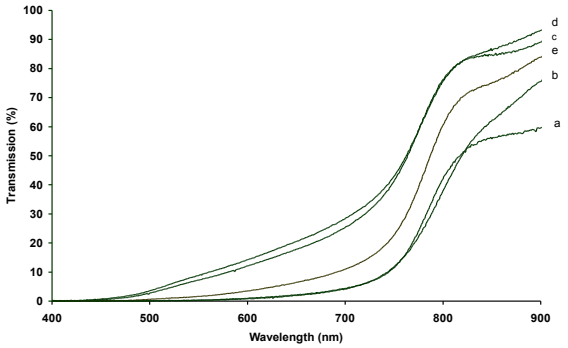


Figure 7. Transmission vs wavelength of light for as-deposited CdTe layers deposited at: (a) 655, (b) 665, (c) 675, (d) 685 and (e) 695 mV vs SCE.

Figure 8 shows the optical transmission spectra for $CdCl_2$ treated CdTe layers, which have been deposited at different voltages. The transmission percentage of layers deposited at 655 mV decreased to ~45% at higher wavelength compared with as-deposited layers. This is most likely be due to the crystallisation of Te in these layers. The transmission percentage of both as-deposited and annealed layers deposited at 685 mV was the same at higher wavelength. This indicates that these layers are close to stoichiometric CdTe.

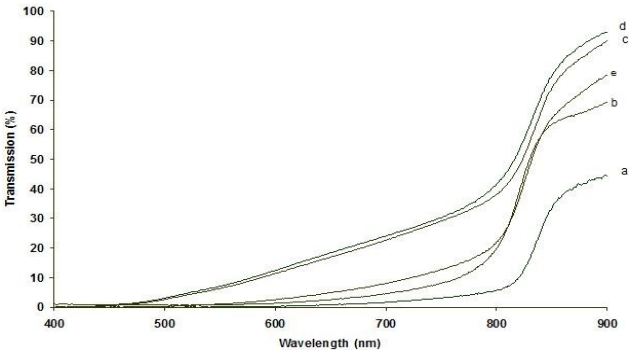


Fig. 8.Transmission vs wavelength of light for CdTe layers deposited at: (a) 655, (b) 665, (c) 675, (d) 685 and (e) 695 mV vs SCE and annealed at 350°C for 20 minutes in air in the presence of $CdCl_2$.

Scanning Electron Microscopy

The surface morphology of CdTe layers was studied by SEM. Figure 9 shows the surface morphology of an as-deposited and annealed film, for layers deposited at 695 mV on a glass/FTO/CdS substrate. It can be seen that annealing causes recrystallisation, which is supported by XRD and optical absorption techniques. The layer after annealing shows a uniform surface covered with larger grains. This suggests that the formation of good quality solar cell material is possible from electroplating ~695 mV and heat treatment in the presence of $CdCl_2$.

In order to reduce the effects of grain boundaries and the defect density of layers, the annealing process is always required. The morphology of annealed CdTe layers deposited at 655, 665, 675, and 685 mV are presented in figure 10. SEM images of the layers deposited at 655 and 665 mV show a different morphology compared to layers deposited at 675 and 685 mV which may suggest a change in composition and crystallization. Pin-holes appear for layers deposited at low cathodic voltages, while the layers deposited at higher cathodic voltages exhibit compact grains without pin-holes. Since the material was expected to be Te-rich for layers deposited at low cathodic voltages as discussed in section LSV, the excess of Te must have sublimed during annealing leaving behind pin-holes. These pin-holes are not helpful and will act as shunting paths reducing device efficiencies.

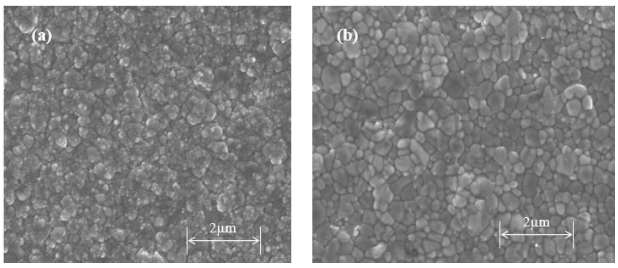
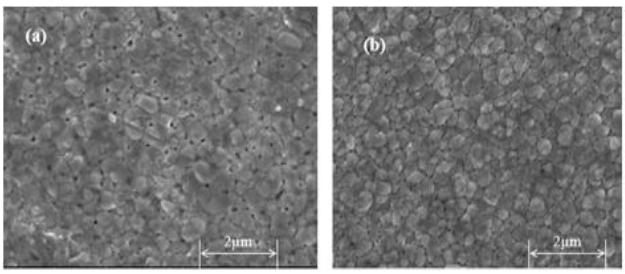


Fig. 9. SEM images of (a) as-deposited and (b) annealed CdTe layers deposited at 695 mV vs SCE.



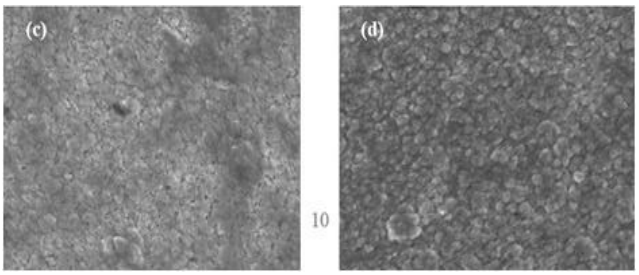
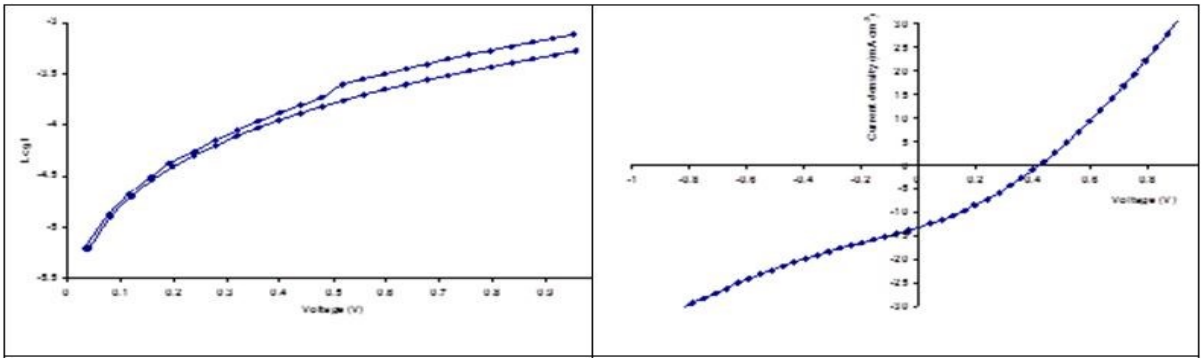


Figure 10: SEM images of heat treated CdTe deposited at: (a) 655, (b) 665, (c) 675, and (d) 685mV vs SCE.

III. CdS/CdTe Device Characterisation

Current-Voltage Measurements

In order to optimise the structure of glass/ FTO/ CdS/ CdTe/Au for devices, current-voltage (I-V) measurements were used to evaluate the device parameters. Before metallisation with Au contacts, CdTe layers were heat treated in the presence of $CdCl_2$ and etched using acidic and alkaline solutions. Typical I-V curves measured in both log-linear under dark condition, and linear-linear under AM1.5 illumination are presented in figure 11 (a) and (b) for CdTe layers grown at two voltages 655 and 695 mV. The cell parameters observed as a function of CdTe growth voltage is given in Table 3. The efficiency gradually increases and gives a maximum of 8.4% for a sample deposited at 695 mV, indicating an electronic quality material composition. Reproducibility of the efficiency with the same growth voltage of 695 mV fluctuated between 4.8 and 8.4%. The changes in the efficiency may be attributed to changes in the Te concentration in the CdTe layer. This structure shows highest values of Jsc and Voc which is due to the most suitable properties of CdTe layers grown at 695 mV. It is clear from the results that at low growth voltage, where CdTe layer is Te rich, devices show poor cell parameters, indicating poor quality of the polycrystalline CdTe. A smaller rectification factor and fill factor was related to CdTe deposited at 655 mV and a larger rectification factor and fill factor related to CdTe grown towards high cathodic voltages. Therefore, this experiment shows that CdTe rich in Te was not suitable for producing good solar cell parameters. Better devices are produced when the material is close to stoichiometric and rich in Cd.



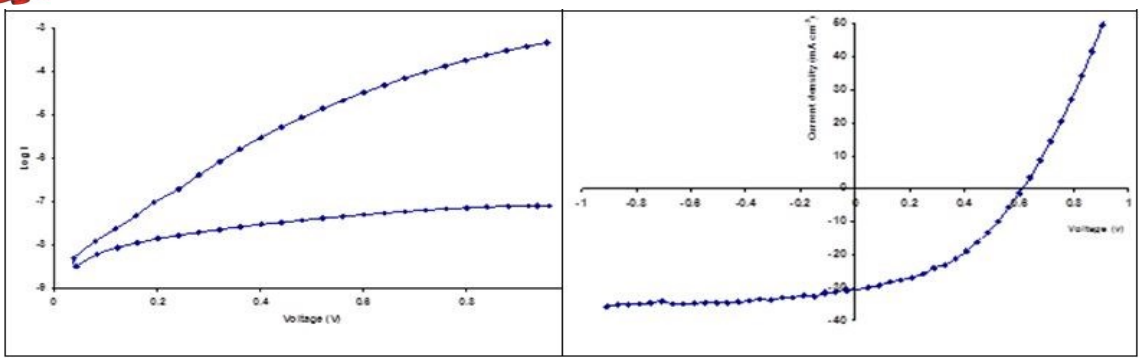


Fig. 11. Log-linear I-V under dark conditions and linear-linear I-V curves under AM1.5 illumination for glass/FTO/ CdS/CdTe/Au structures for CdTe layers deposited at 655 mV (upper two panels) and 695 mV (lower two panels). Note the drastic change of I-V curves when CdTe change from Te-richness to Cd-richness. Figure 12 shows the variation of cell parameters as a function of the CdTe growth voltage.

Table 3. Device parameters of glass/FTO/CdS/CdTe/Au as a function of the CdTe growth voltage.

V_g(mV)	R_F	V_{oc} (V)	J_{sc} (mA cm^{-2})	FF	η (%)
655	$10^{0.2}$	0.44	13.0	0.30	1.7
665	$10^{2.9}$	0.52	15.5	0.33	2.7
675	$10^{3.4}$	0.56	8.4	0.39	1.8
685	$10^{5.3}$	0.52	12.6	0.48	3.0
695	$10^{3.7}$	0.64	31.0	0.41	8.4

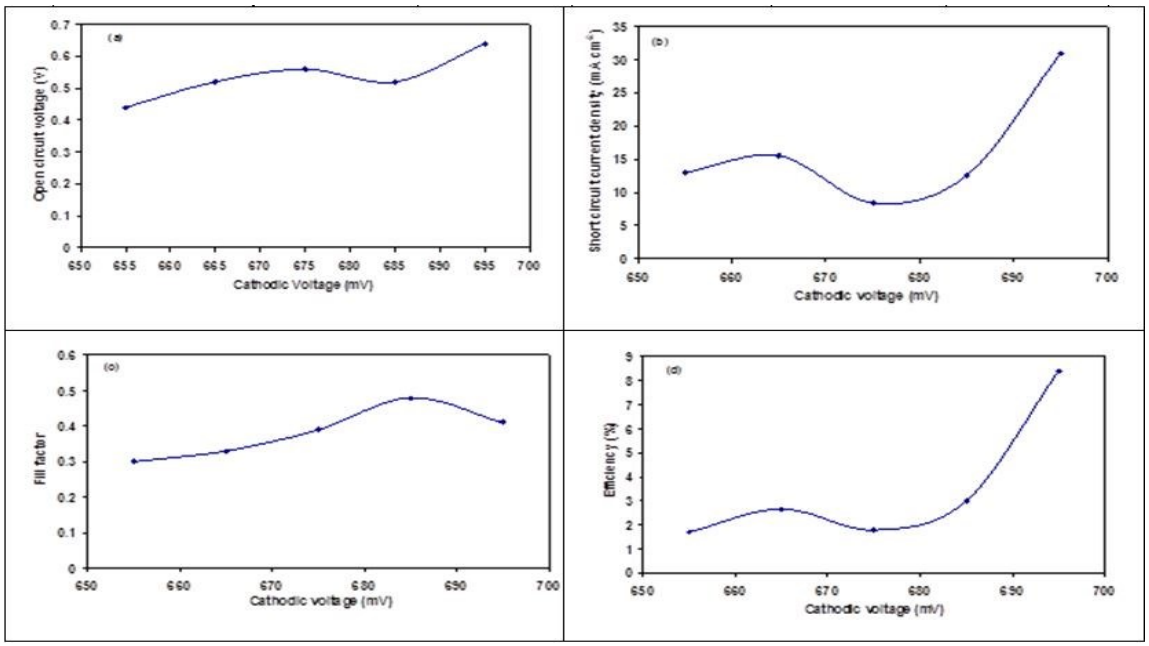


Fig. 12. (a) open circuit voltage, (b) short circuit current density, (c) fill factor and (d) efficiency as a function of the CdTe growth voltage.

IV. Conclusions

The results presented in this paper show that chlorine treatment has a beneficial effect on the semiconductor properties. The CdTe layer was deposited using a three electrode system with growth voltages of 655, 665, 675, 685 and 695 mV vs SCE and annealed at 350°C for 20 minutes in air. As-deposited and annealed CdTe have been studied using XRD, optical absorption, SEM and I-V measurements to assess the semiconductor properties and devise performance. CdTe layers grown have cubic crystal structure with (111) preferred orientation, and their energy bandgap is close to that of the bulk material (~1.50 eV). The CdTe layers grown at low cathodic voltages are rich in Te, and produce very poor devices. As the deposition voltage increase, Cd content increases, and material layer get closer to stoichiometric and Cd-rich region. Although the optimisation need further work, the layers deposited at 695 mV show better device quality material, producing device parameters of V_{oc} = 640 mV, J_{sc} = 31 mAcm^{-2}, FF = 0.42 and η = 8.4%. The work is continuing to further optimise the growth conditions and hence increase the device parameters.

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